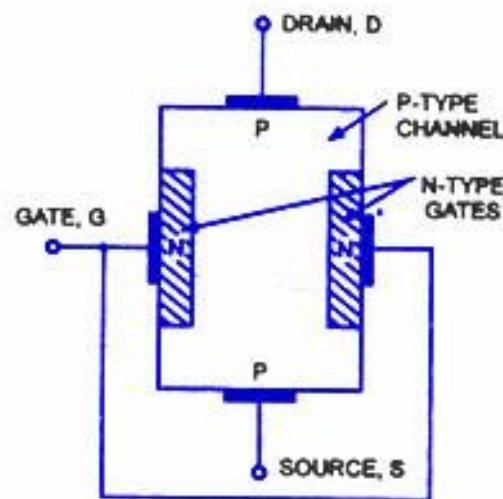
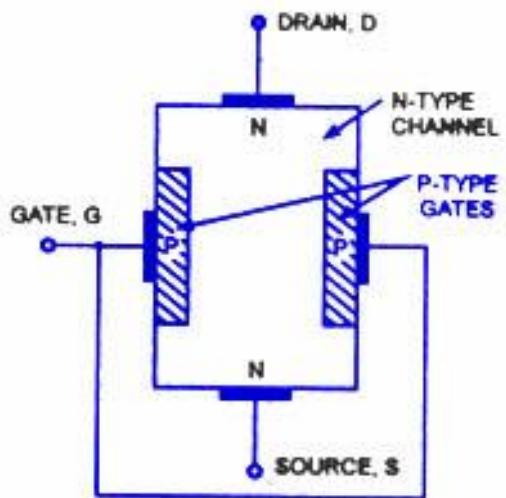
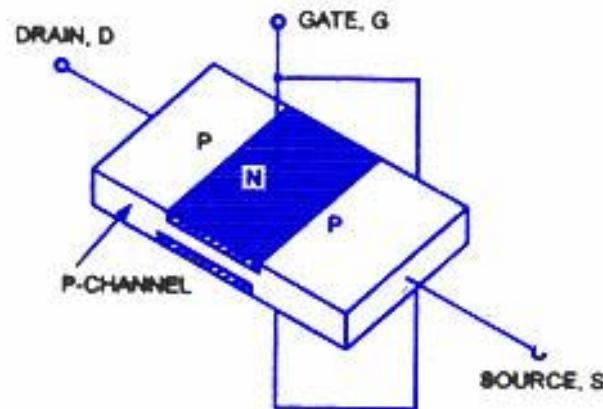
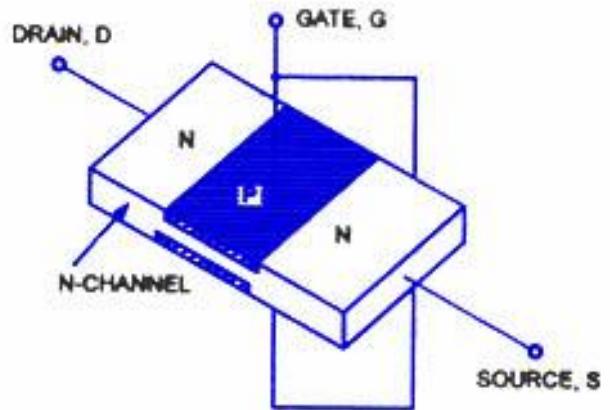


FET

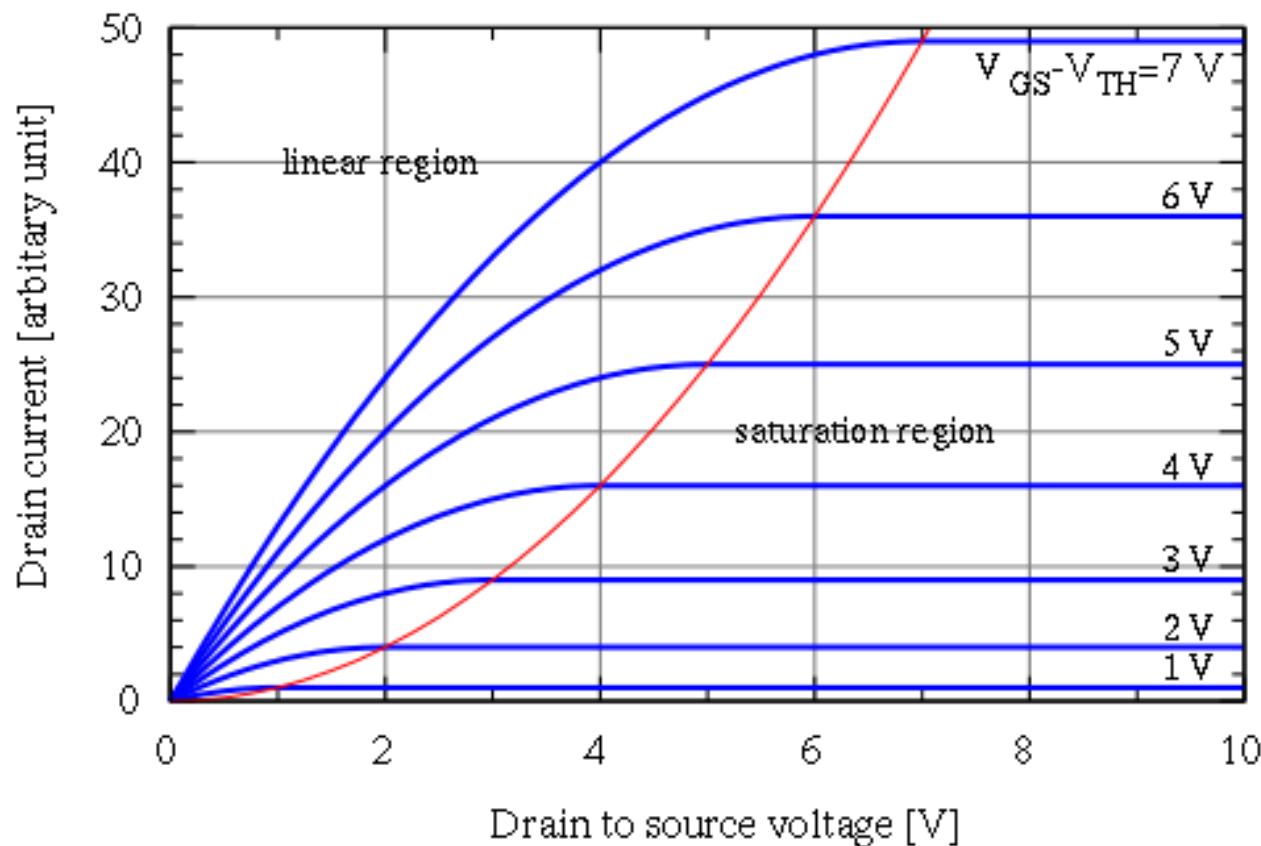


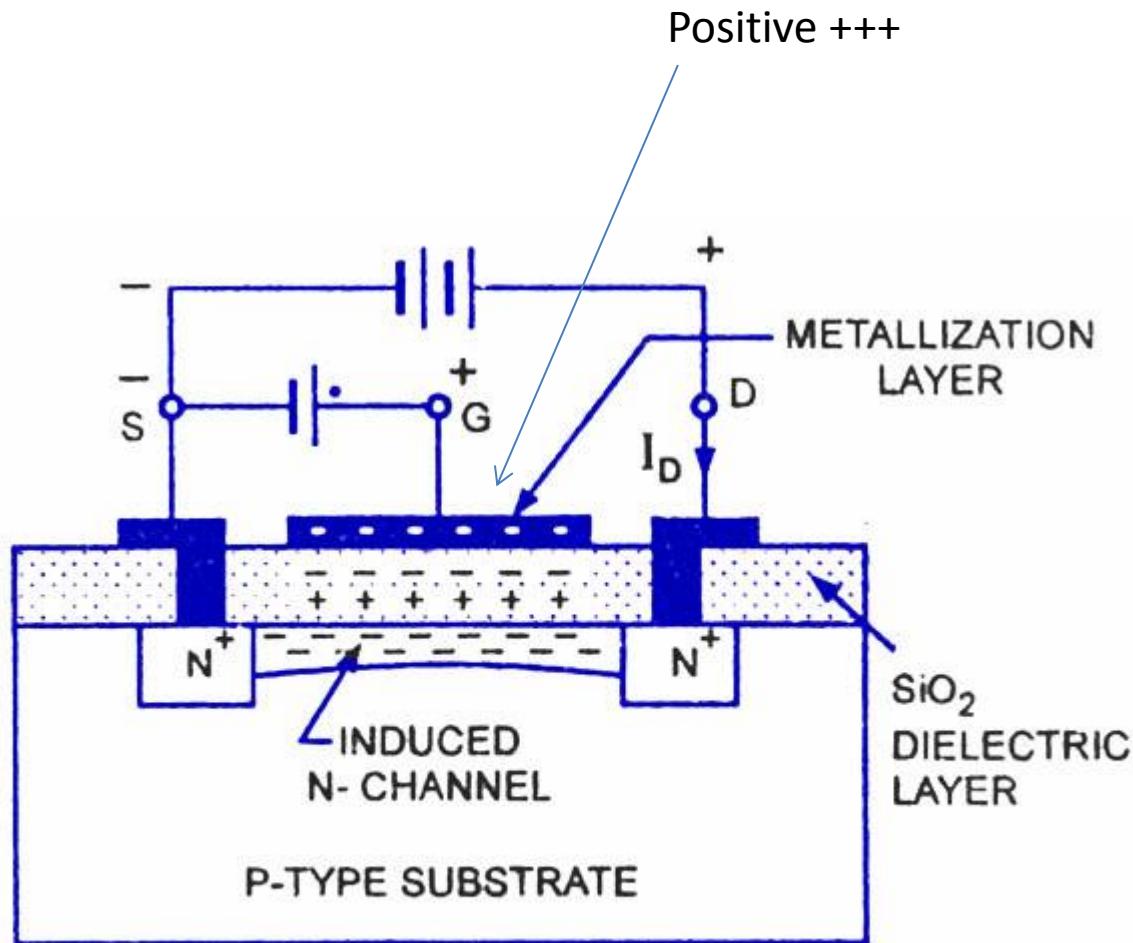
N-Channel JFET

P-Channel JFET

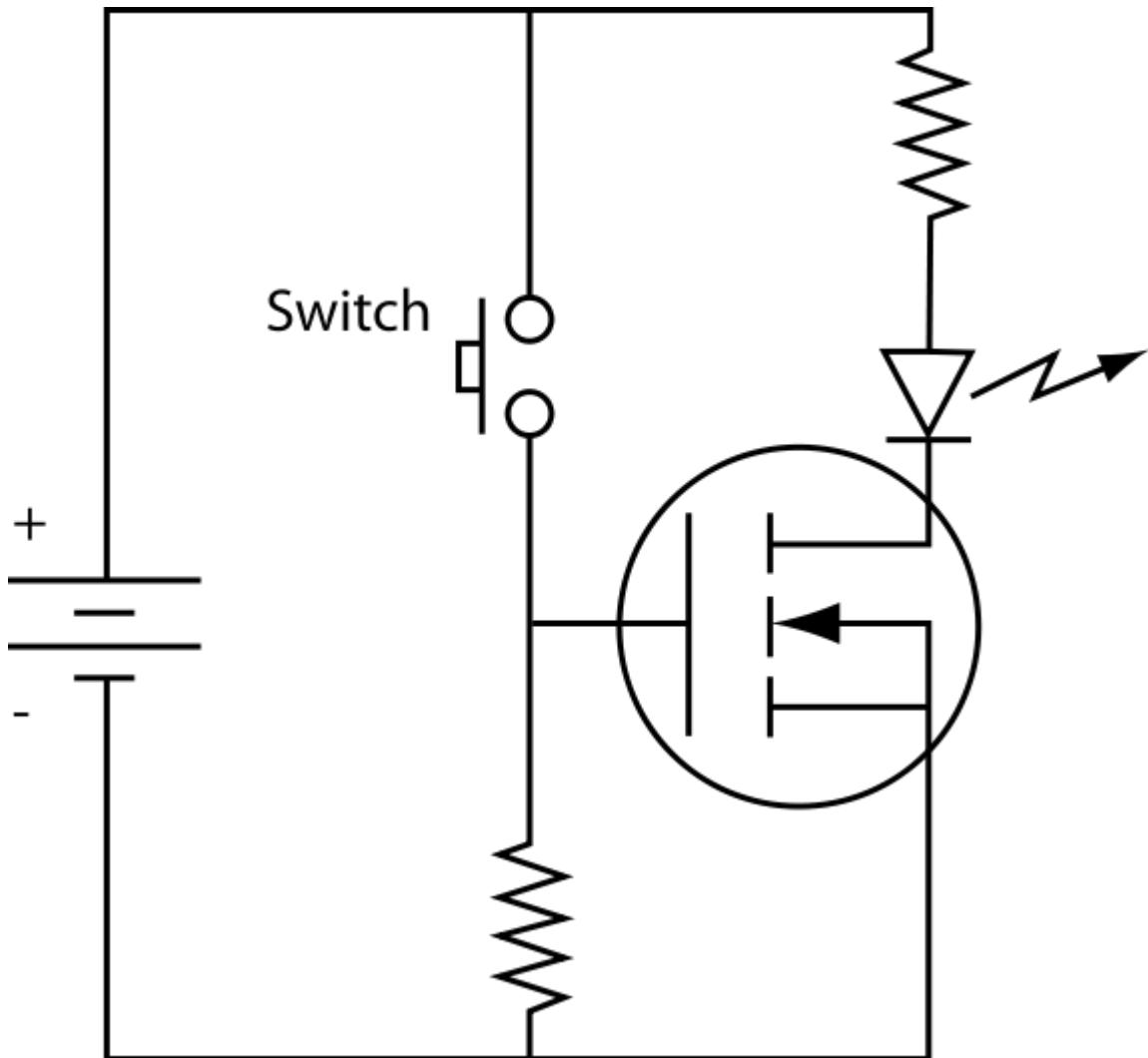
JFETs

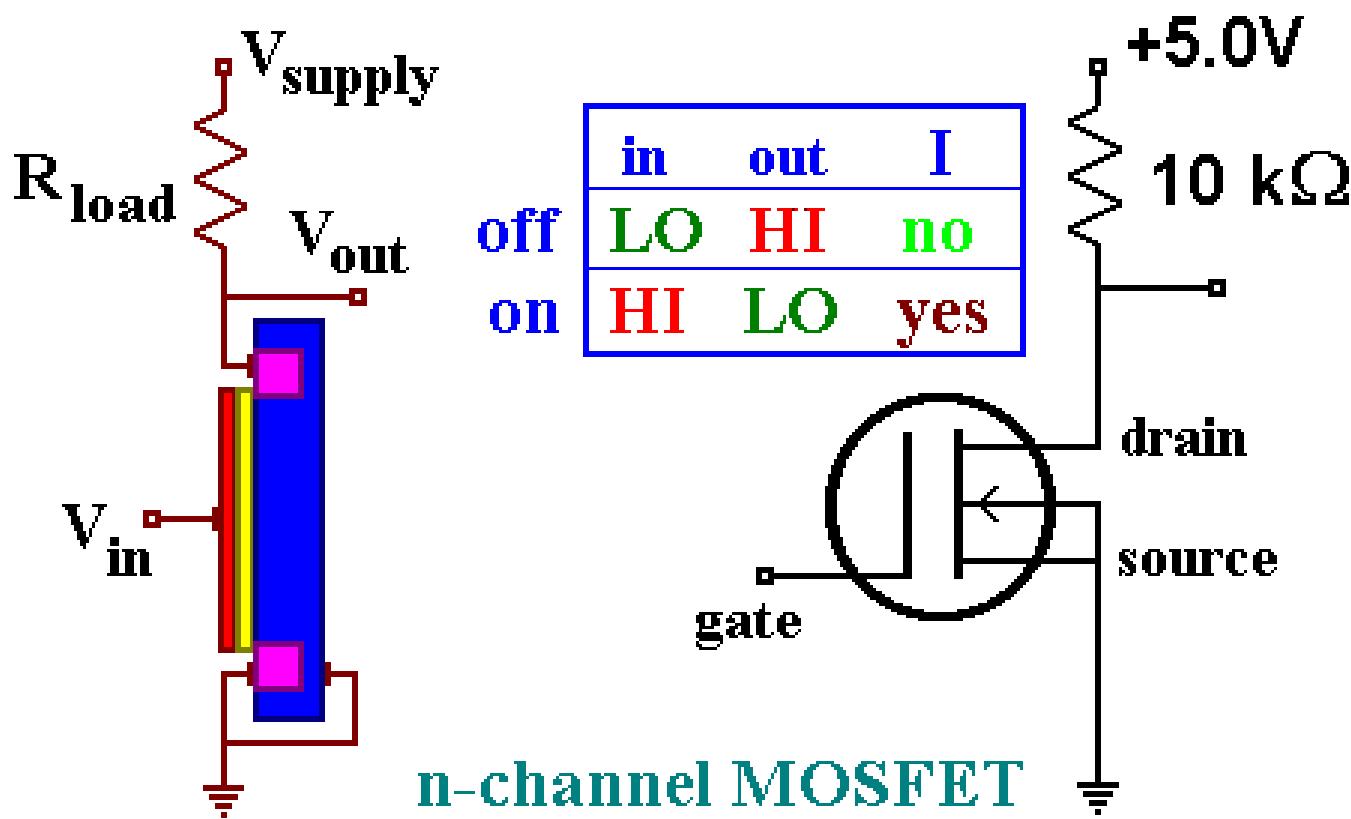
IDS versus VDS Curves



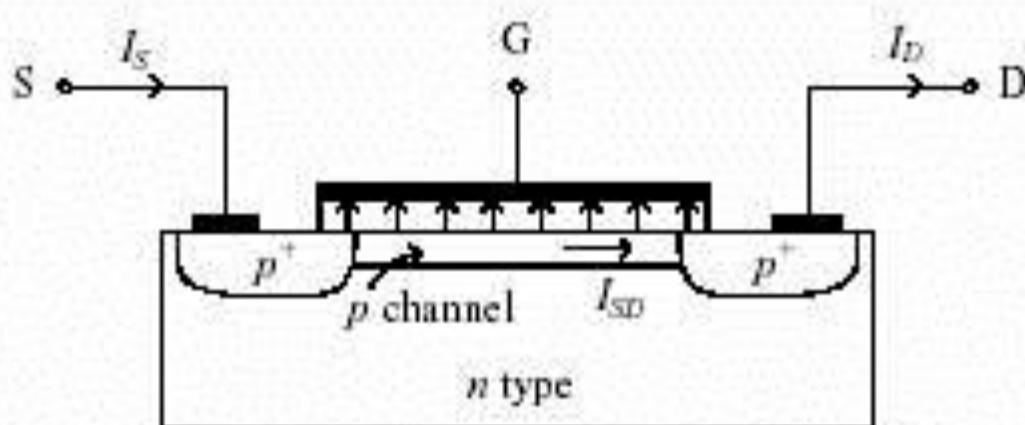


Operation of N-Channel E-MOSFET



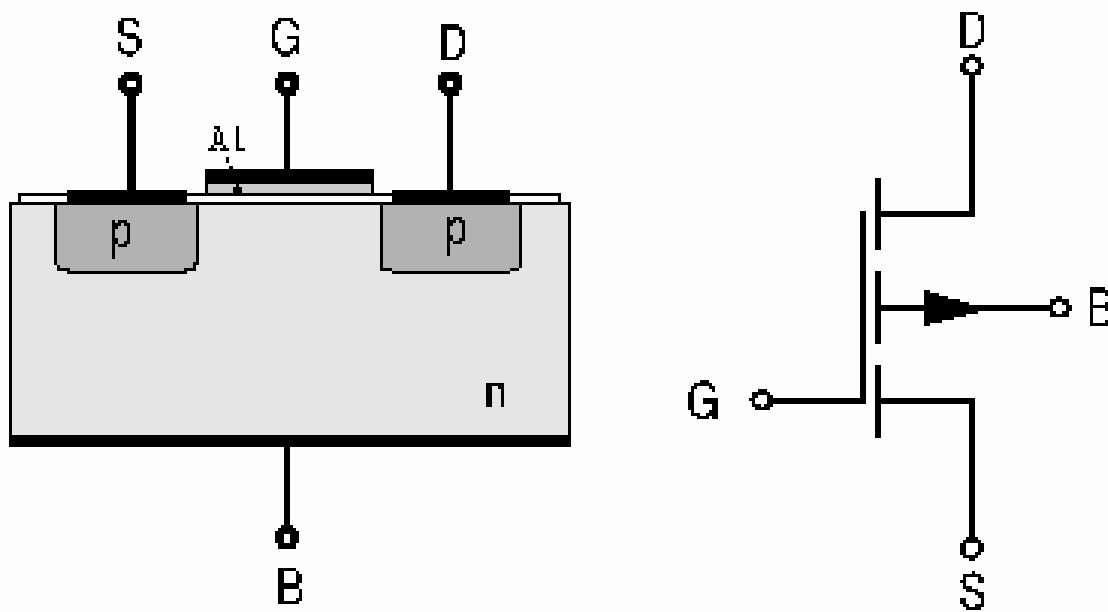


P channel MOS



P Channel MOS

MOS canal p à enrichissement

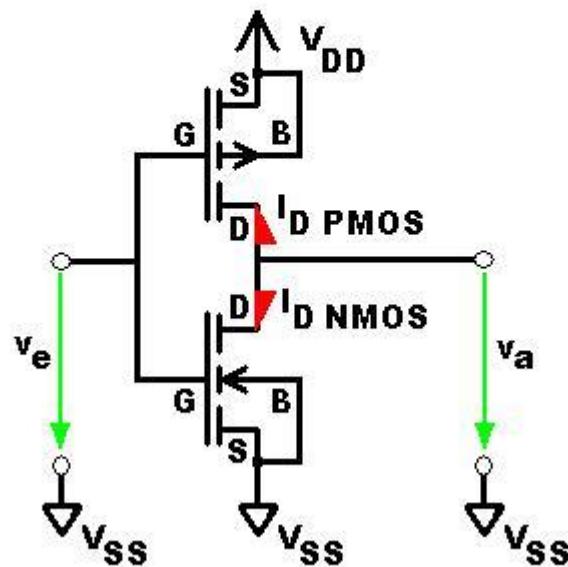


CMOS

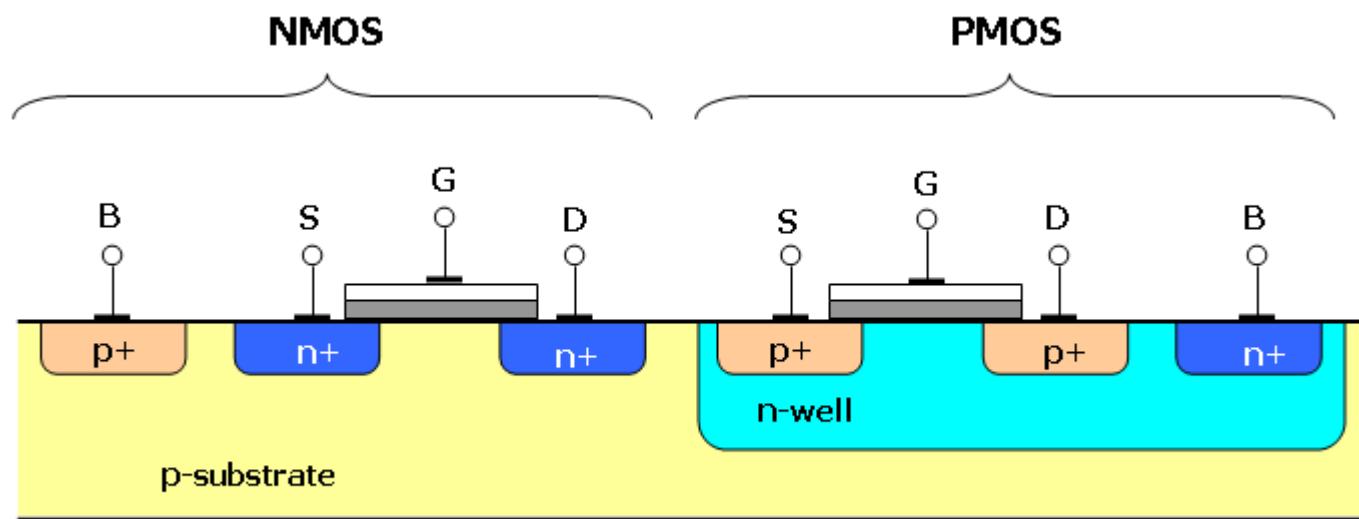
Drain / Source Gebiete am Beispiel CMOS Inverter

PMOS enhancement ($V_{TH} < 0 \text{ V}$)

NMOS enhancement ($V_{TH} > 0 \text{ V}$)

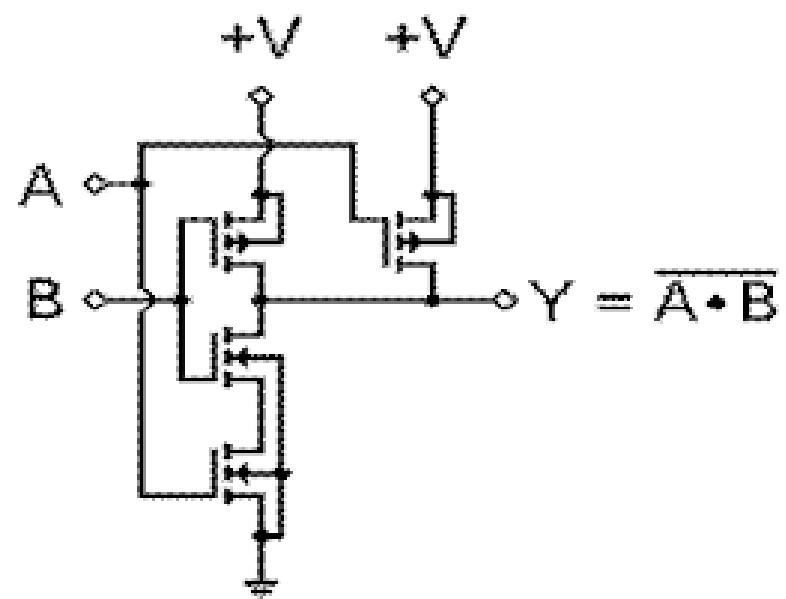
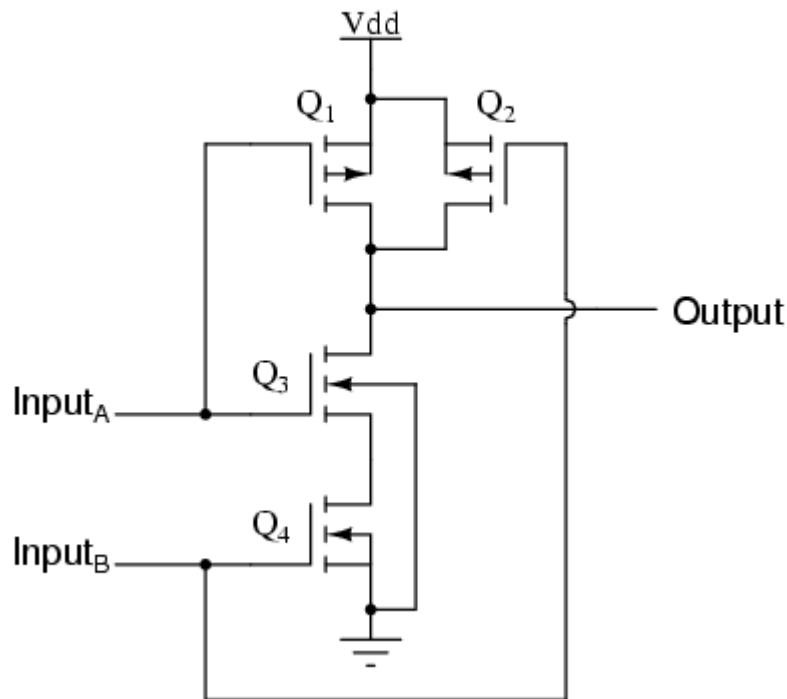


CMOS



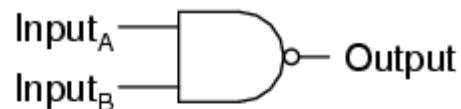
CMOS

CMOS NAND gate



CMOS Digital family

2-input NAND gate



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Equivalent gate circuit



FIM