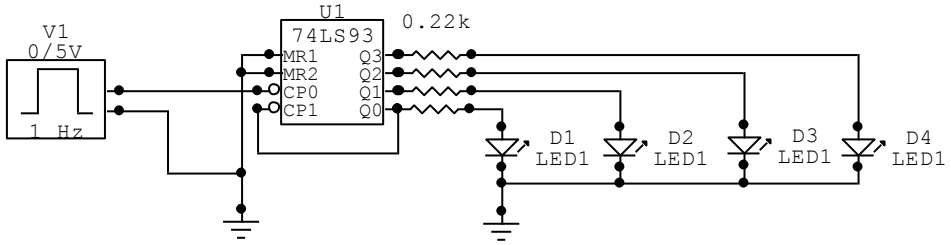
F541 Aula 3

CONTADOR BINÁRIO

Monte no protoboard o circuito abaixo.

Aplique os pulsos de clock e veja as correspondentes sequencias de acionamento dos LEDs.

Use o osciloscópio para ver os sinais colocando o pulso do gerador no Triger externo do osciloscópio. Você pode “resetar” os FF sempre que acionar o R (Reset) dos FF.



Para o 74LS93:

VCC = PIN 5
GND = PIN 10
NC = PIN 4, 6, 7, 13

Inicialmente use f=1Hz. Depois use 100Hz e observe ossinais em cada terminal Qi.

MOTOROLA

DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

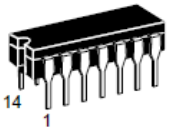
SN54/74LS90
SN54/74LS92
SN54/74LS93

DECADE COUNTER; DIVIDE-BY-TWELVE COUN 4-BIT BINARY COUNTE

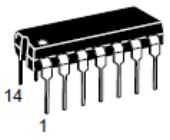
LOW POWER SCHOTTK

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects



J SUFF
CERAM
CASE 63



N SUFF
PLAST
CASE 64

D SUFF
SOIC
CASE 751

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	0.5 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	0.5 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5 (2.5) U.L.

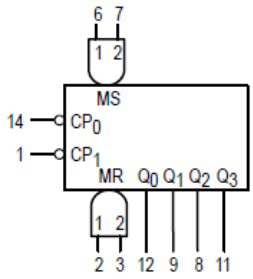
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.
d. To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

ORDERING INFORMATIO

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

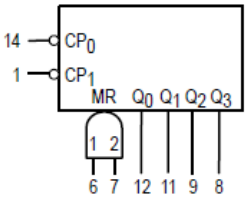
LOGIC SYMBOL

LS90



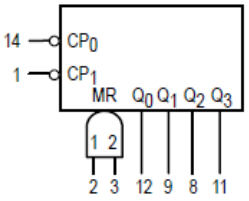
V_{CC} = PIN 5
GND = PIN 10
NC = PINS 4, 13

LS92



V_{CC} = PIN 5
GND = PIN 10
NC = PINS 2, 3, 4, 13

LS93



V_{CC} = PIN 5
GND = PIN 10
NC = PIN 4, 6, 7, 13

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 2004

MM74C93
4-Bit Binary Counter

General Description

The MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}, and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

All inputs are protected against static discharge damage.

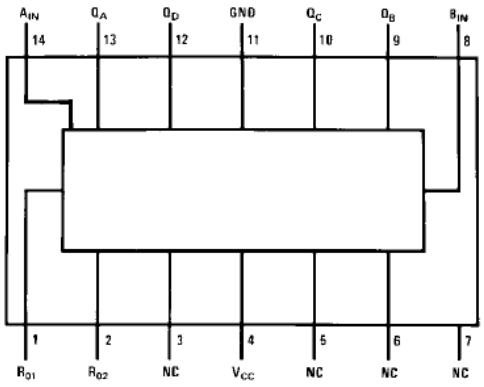
Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power compatibility:
  Fan out of 2 TTL driving 74L
- The MM74C93 follows the MM74L93 Pinout

Ordering Code:

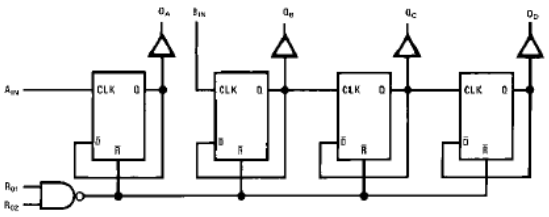
Order Number	Package Number	Package Description
MM74C93N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Top View

Logic Diagram



Truth Table

4-Bit Binary Counter Binary Count Sequence

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B for binary count sequence.
H = HIGH Level
L = LOW Level
X = Irrelevant