# Timer 555. Monostable, PWM

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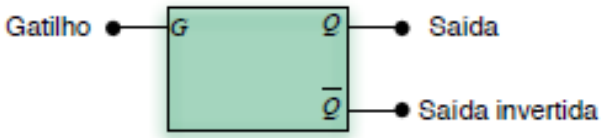
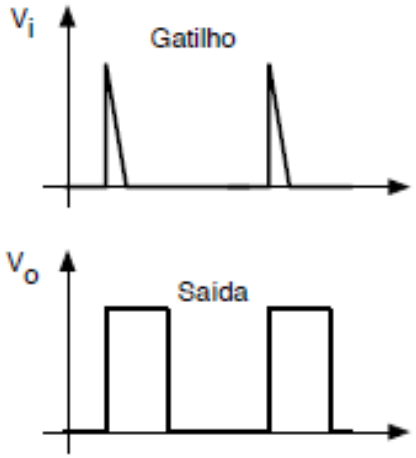
F540

# Multivibradores Monoestáveis

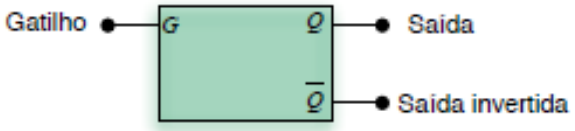
- ✓ **Apresenta somente um estado estável;**
- ✓ **Estimulo de gatilho é necessário para o estado instável;**
- ✓ **O estado instável permanece por um período determinado.**

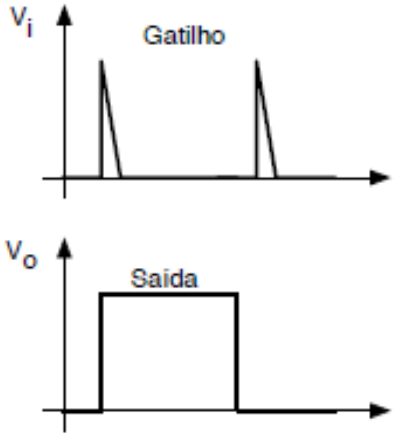


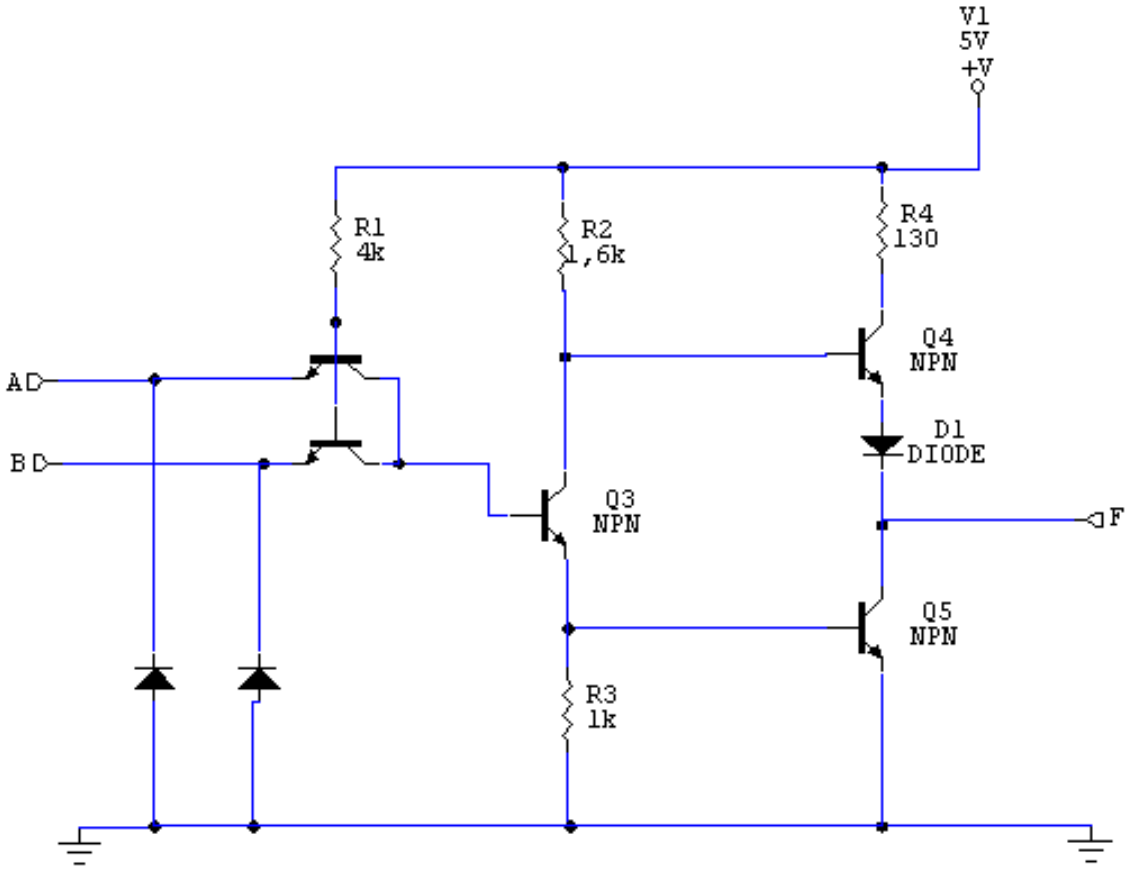
# Multivibradores Biestáveis

- ✓ **Apresenta dois estados estáveis;**
- ✓ **Estimulo de gatilho é necessário para o a troca de estados;**
- ✓ **A troca dos estado ocorre pelo disparo do gatilho.**



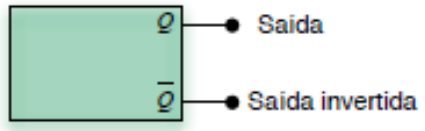
# Basic NAND Gate

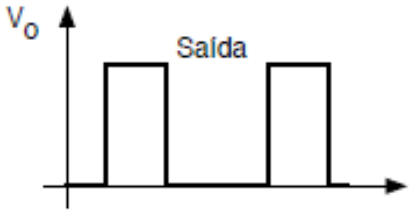



| A/V | B/V | F/V |
|---|---|---|
| 0 | 0 | 5 |
| 0 | 5 | 5 |
| 5 | 0 | 5 |
| 5 | 5 | 0 |

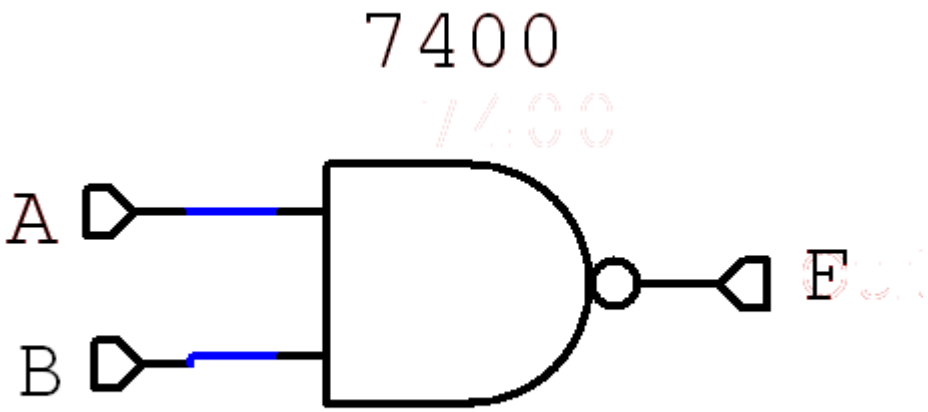
## Multivibradores Astáveis

- ✓ Não apresenta estado estável;
- ✓ Não existe a necessidade de disparo de gatilho;
- ✓ Os estados variam constantemente, gerando um sinal oscilante na saída.



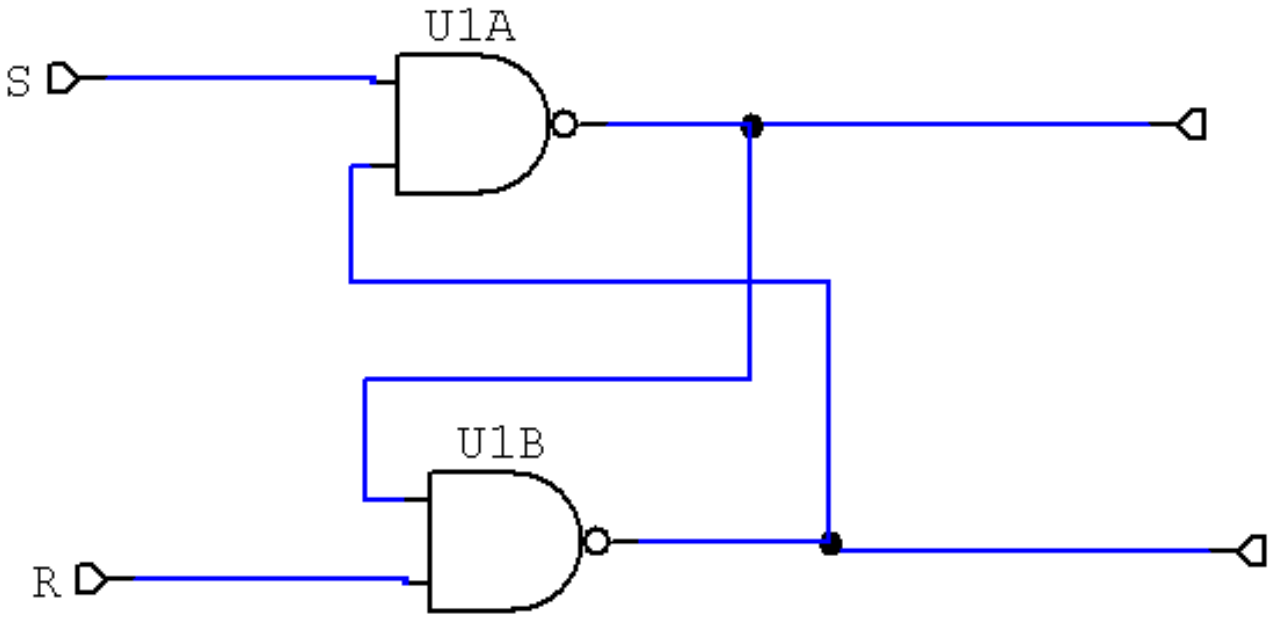



# Nand gate (2 inputs)



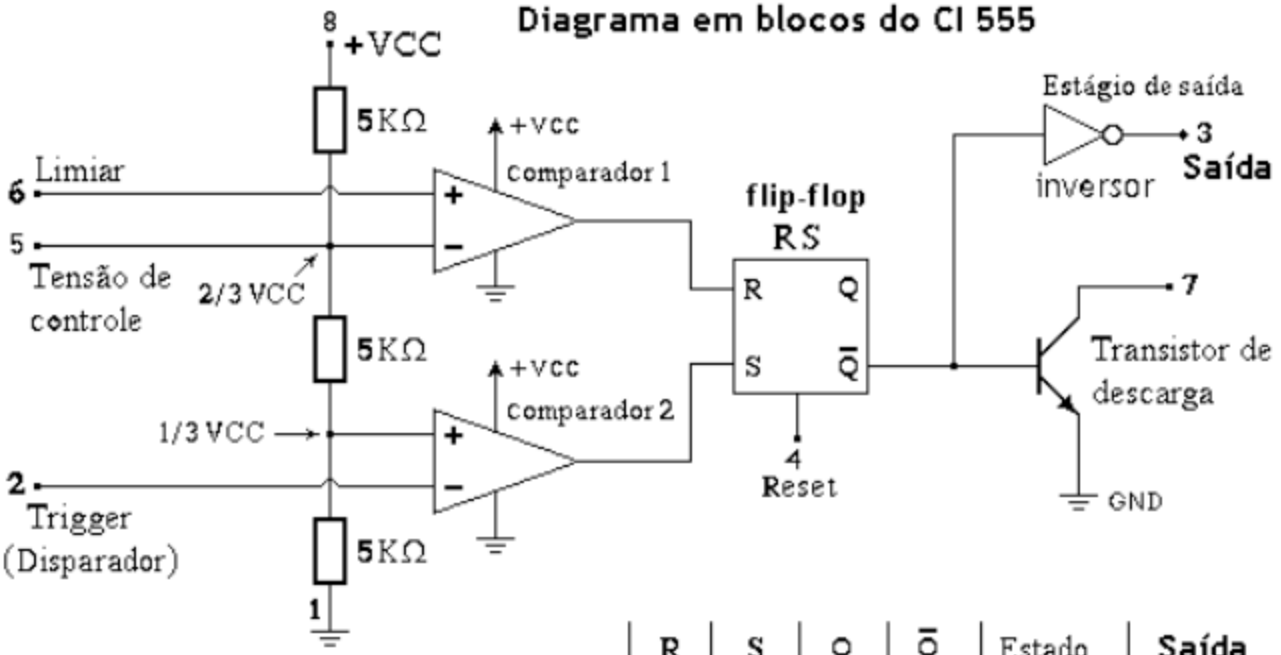

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# Flip Flop SR




| R | S | Q | Q´ |
|---|---|---|---|
| 1 | 1 | Q | Q´ |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |

# Circuito Integrado 555




V 6 < 2 / 3 VCC ⇒ R = 0
V 2 < 1 / 3 VCC ⇒ S = 1

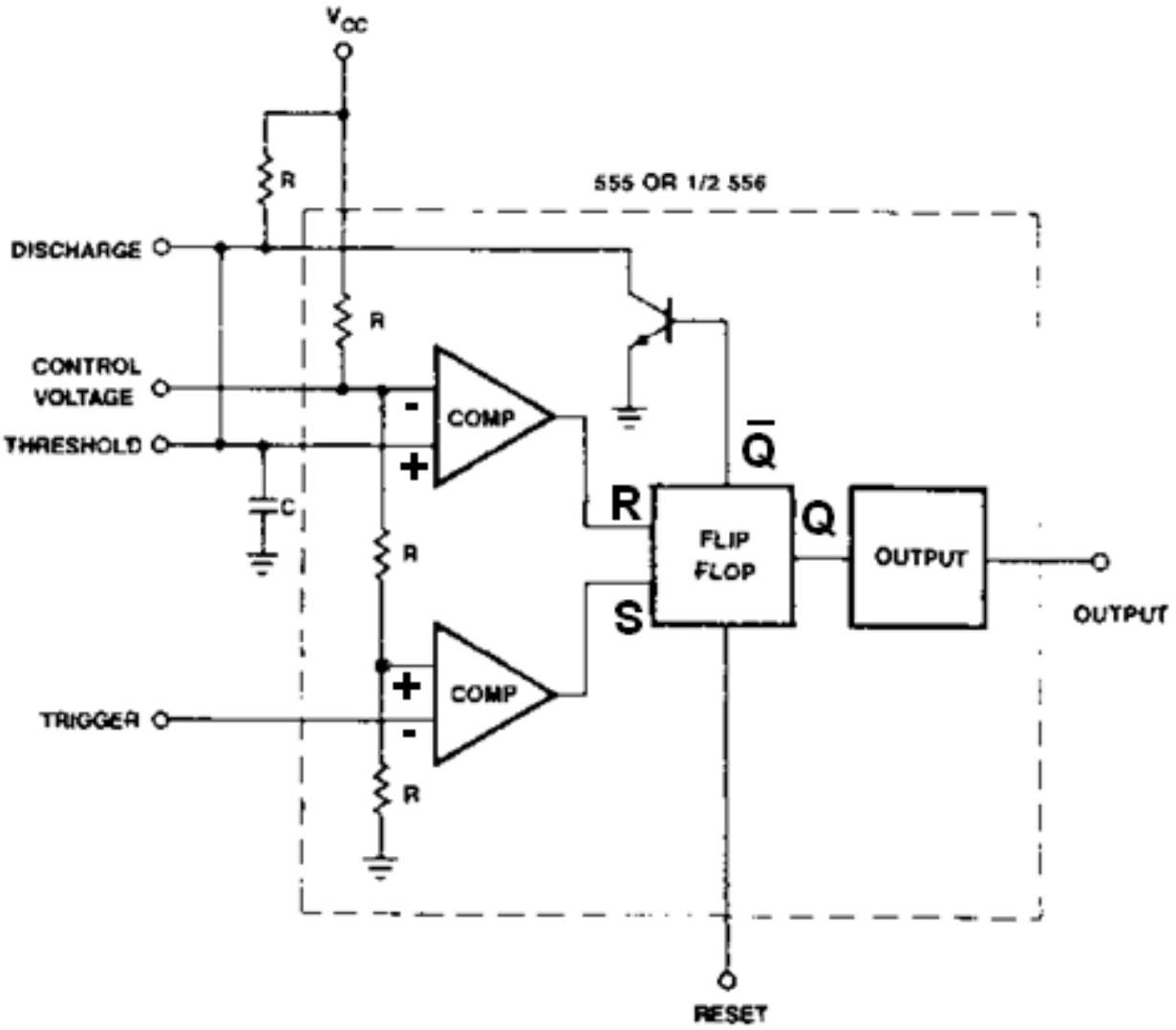
V 6 > 2 / 3 VCC ⇒ R = 1
V 2 > 1 / 3 VCC ⇒ S = 0

V6 => tensão no pino 6
V2 => tensão no pino 2

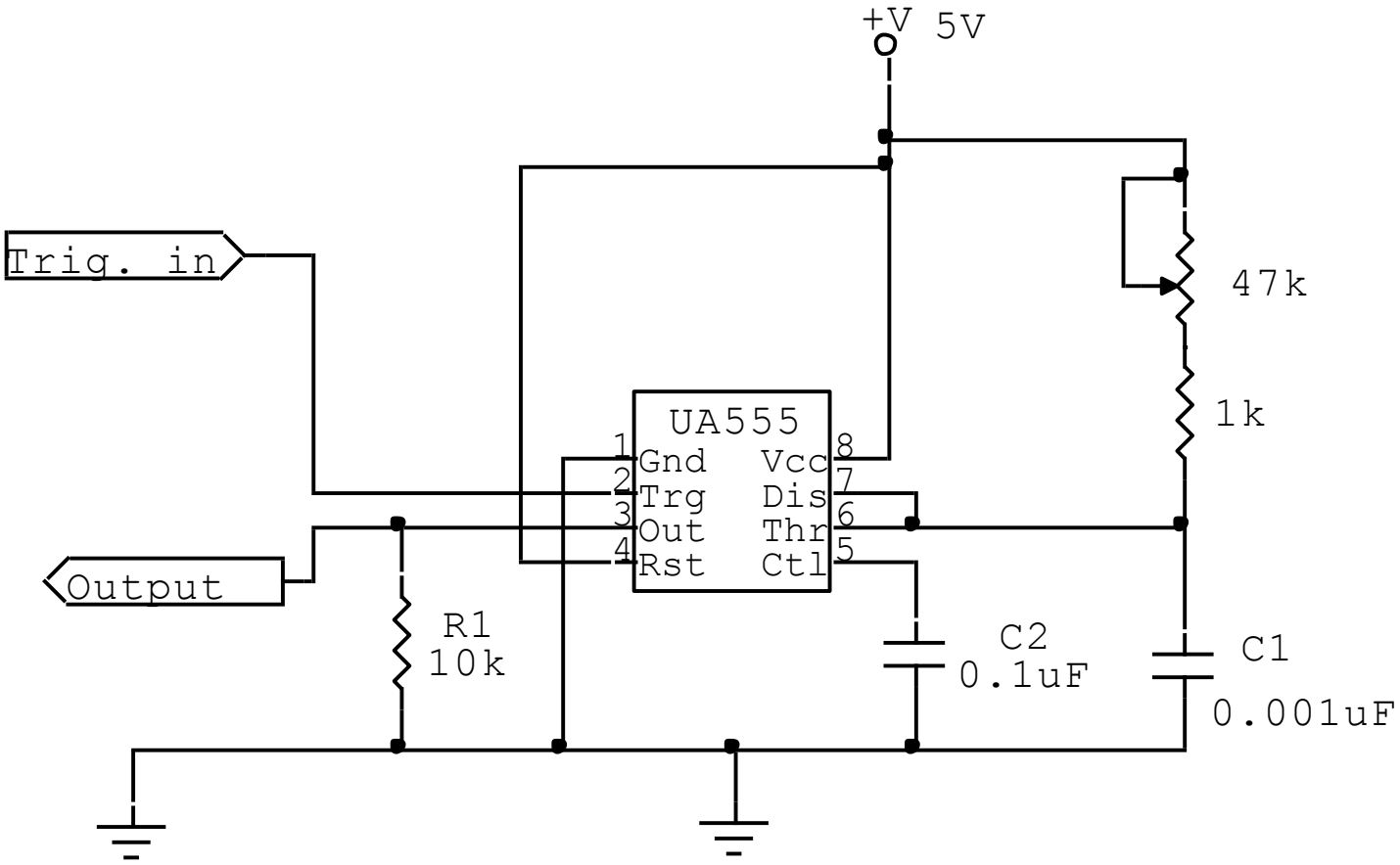
| R | S | Q | $\bar{Q}$ | Estado | Saída |
|---|---|---|---|---|---|
| 0 | 0 | Não muda | | Hold | não muda |
| 0 | 1 | 1 | 0 | Set | 1 |
| 1 | 0 | 0 | 1 | Reset | 0 |
| 1 | 1 | 0 | 0 | Proibido | 1 |

flip-flop

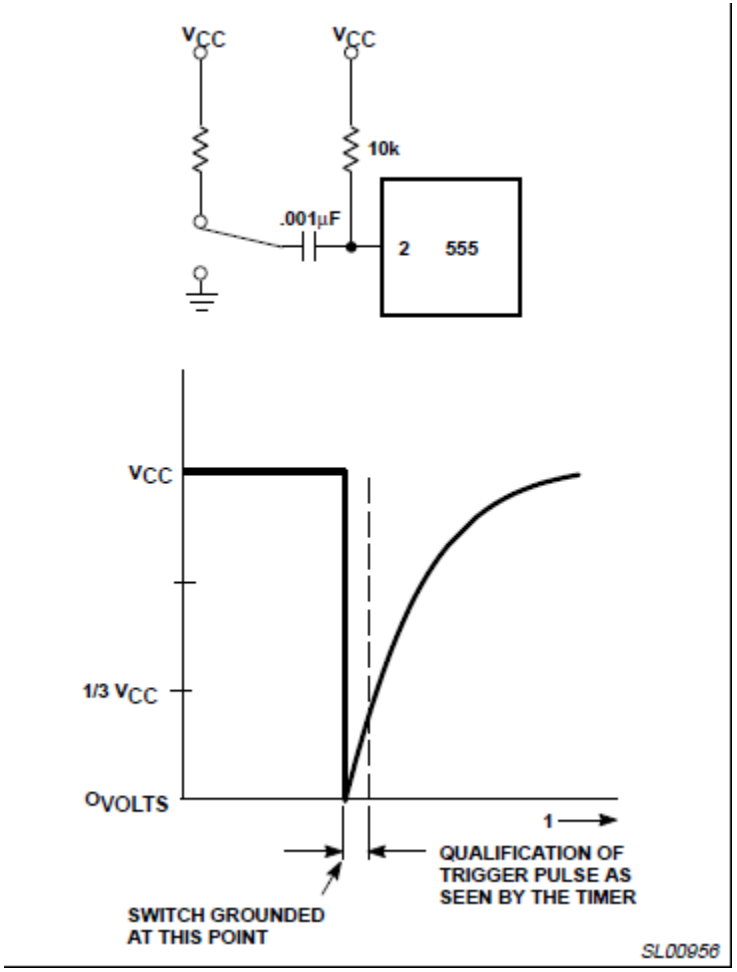
**The 555 timer consists of two voltage comparators (op amplifiers), a bistable flip-flop, a discharge transistor, and a resistor divider network. See the block form in Figure. A Monostable circuit.**



# Negative edge  triggered Mono-stable circuit. 555



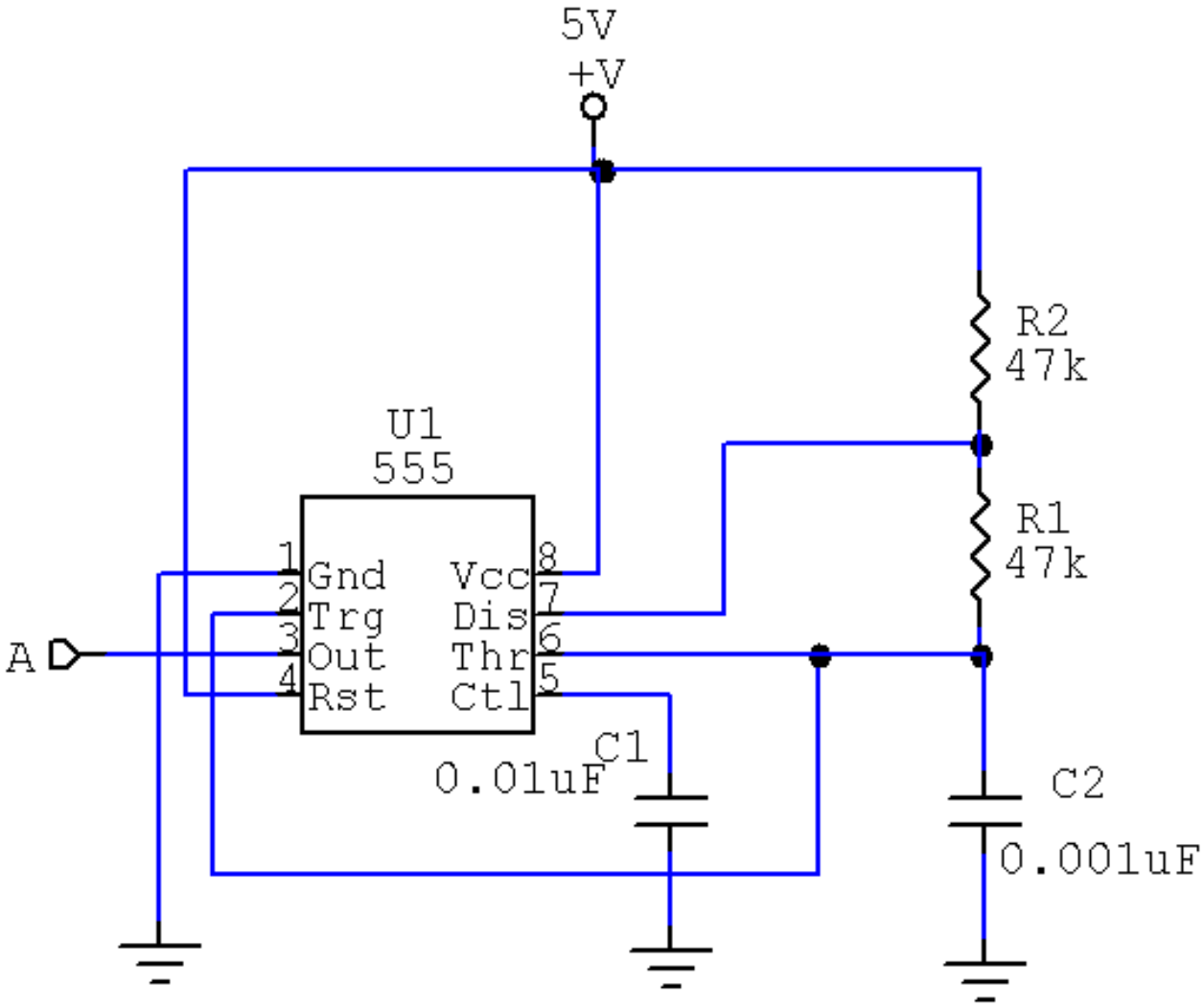
***By AC coupling the trigger , a short negative-going pulse is achieved when the trigger signal goes to ground*.**

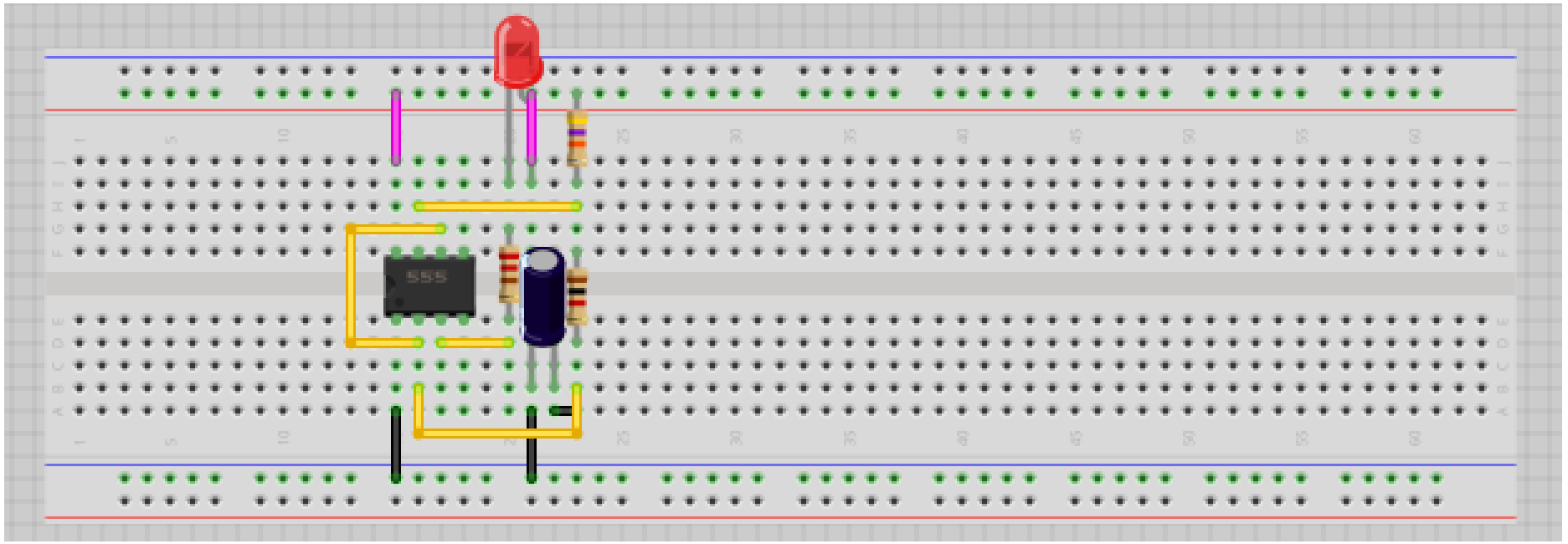


*Uppon aplication of the negative pulse to pin 2, the FF is Set which releases de schort circuit across the external capacitor C and drives the output High. The capacitor charges in a time 1.1$R_A$ C. When the voltage across the capacitor reaches 2/3 VCC, the comparator resets the FF discharging C and output goes Low.*

**Signetics Application Note AN170**

# Astable operation- 555

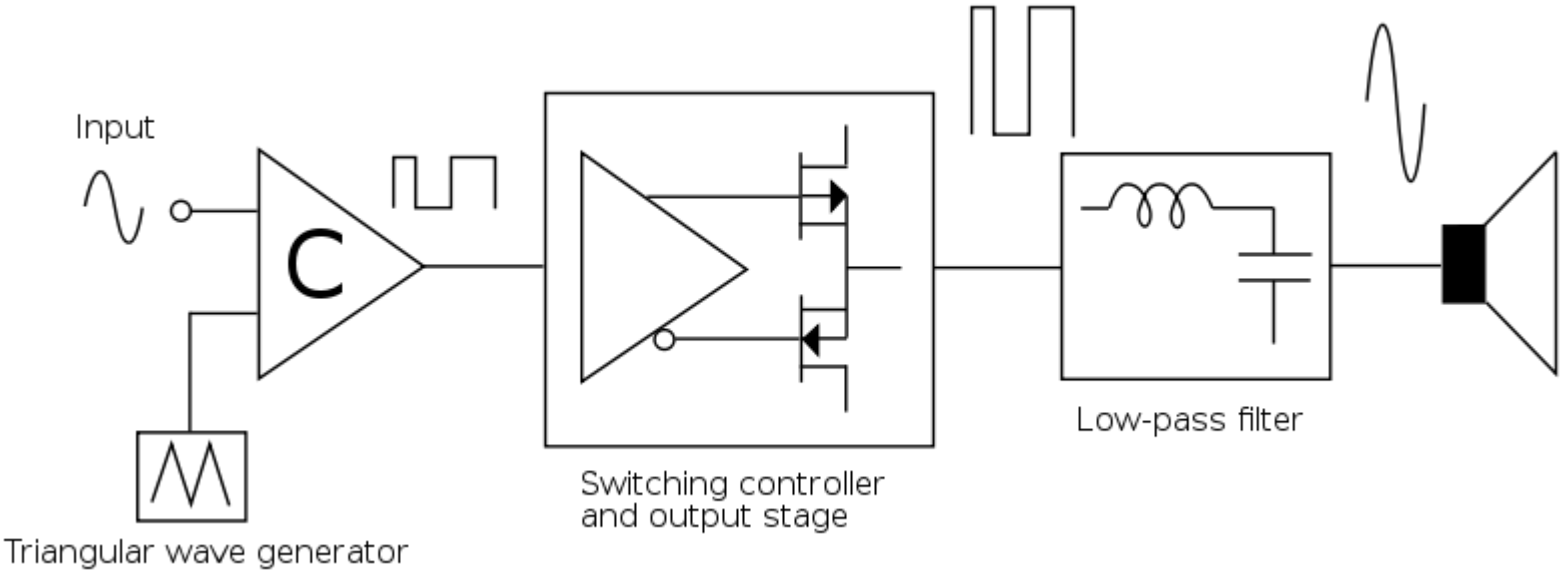



555

# PWM

- In this configuration, the monostable circuit is triggered by the astable circuit.
- By changing the variable resistor R=47k we change the pulse width.
- By applying a 2V sinusoidal modulating voltage to pin 5 of the mono, we modulate the pulse width.

# This PWM is used in Class d amplifier.



# Fim