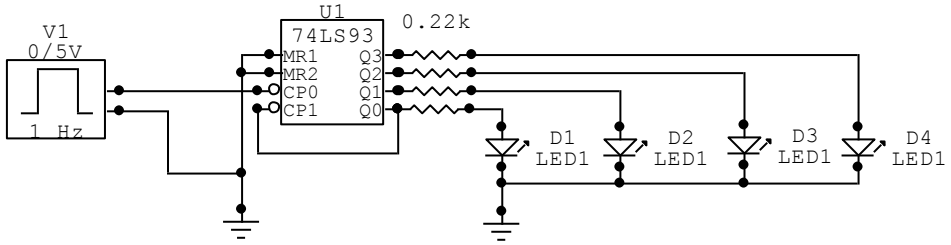
F541 Aula 3

CONTADOR BINÁRIO

Monte no protoboard o circuito abaixo.

Aplique os pulsos de clock e veja as correspondentes sequências de acionamento dos LEDs.

Use o osciloscópio para ver os sinais colocando o pulso do gerador no Triger externo do osciloscópio. Você pode "resetar" os FF sempre que acionar o R (Reset) dos FF.



Para o 74LS93:

VCC = PIN 5
GND = PIN 10
NC = PIN 4, 6, 7, 13

Inicialmente use f=1Hz. Depois use 100Hz e observe ossinais em cada terminal Qi.

MOTOROLA

DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

SN54/74LS90
SN54/74LS92
SN54/74LS93

DECADE COUNTER;
DIVIDE-BY-TWELVE COUNTER;
4-BIT BINARY COUNTER

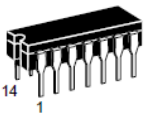
LOW POWER SCHOTTKY

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

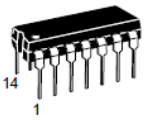
- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	0.5 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	0.5 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.
d. To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

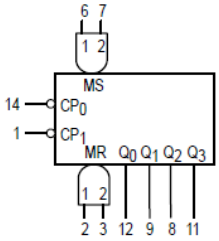
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

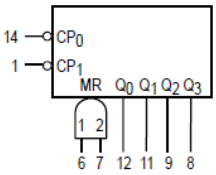
LOGIC SYMBOL

LS90



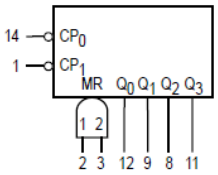
V_{CC} = PIN 5
GND = PIN 10
NC = PINS 4, 13

LS92



V_{CC} = PIN 5
GND = PIN 10
NC = PINS 2, 3, 4, 13

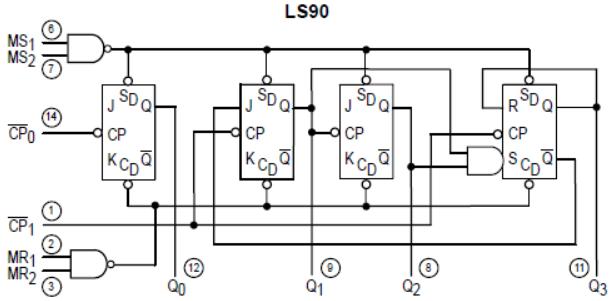
LS93



V_{CC} = PIN 5
GND = PIN 10
NC = PIN 4, 6, 7, 13

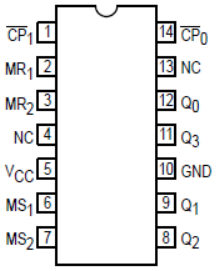
LOGIC DIAGRAM

LS90



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

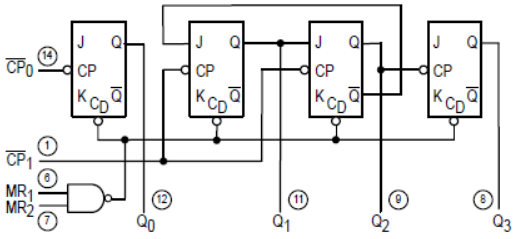


NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

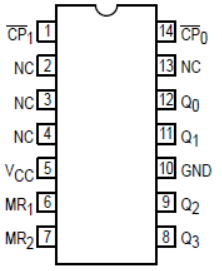
LOGIC DIAGRAM

LS92



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

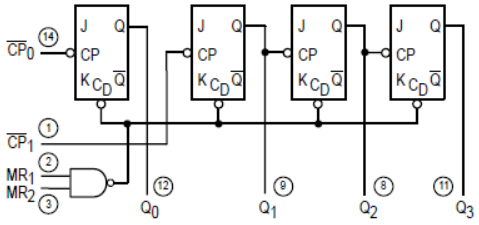


NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

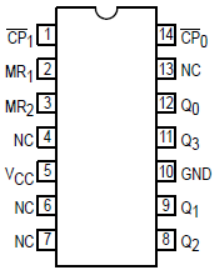
LOGIC DIAGRAM

LS93



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

National Semiconductor

July 1992

DM5490/DM7490A, DM7493A Decade and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A and divide-by-eight for the 93A.

All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine's complement applications.

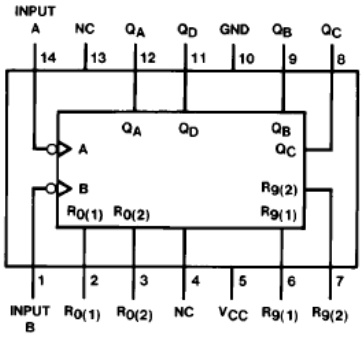
To use their maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- Typical power dissipation
  - — 90A 145 mW
  - — 93A 130 mW
- Count frequency 42 MHz

Connection Diagrams

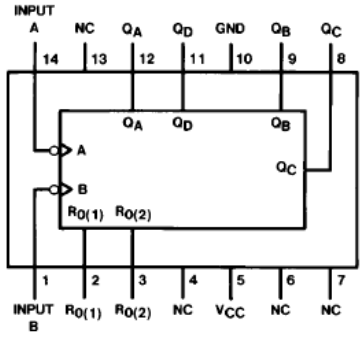
Dual-In-Line Package



TL/F/6533–1

Order Number DM5490J, DM5490W or DM7490AN
See NS Package Number J14A, N14A or W14B

Dual-In-Line Package



TL/F/6533–2

Order Number DM7493AN
See NS Package Number N14A

Function Tables (Note D)

90A
BCD Count Sequence
(See Note A)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

90A
BCD Bi-Quinary (5-2)
(See Note B)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

93A
Count Sequence
(See Note C)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

90A
Reset/Count Function Table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L		COUNT		
L	X	L	X		COUNT		
L	X	X	L		COUNT		
X	L	L	X		COUNT		

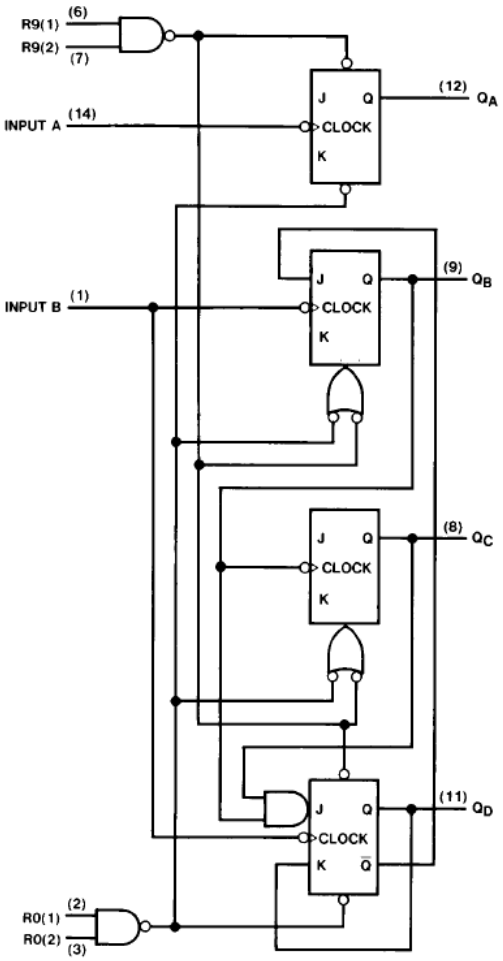
93A
Reset/Count Function Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X		COUNT		
X	L		COUNT		

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for bi-quinary count.
Note C: Output Q_A is connected to input B.
Note D: H = High Level, L = Low Level, X = Don't Care.

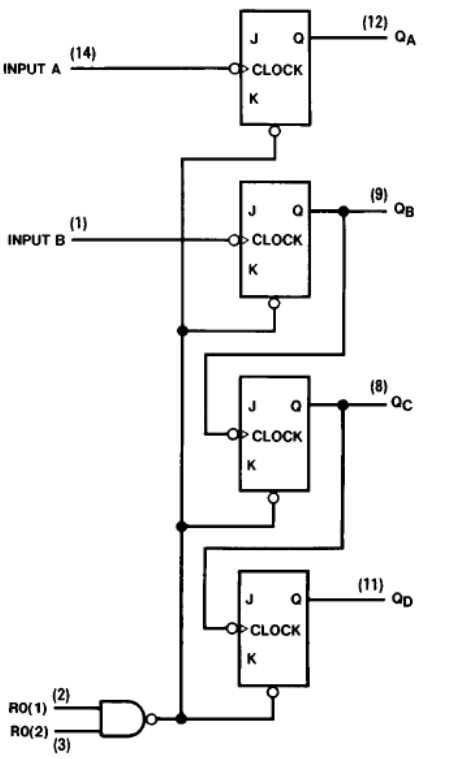
Logic Diagrams

90A



TL/F/6533–3

93A



TL/F/6533–4

The J and K inputs shown without connection are for reference only and are functionally at a high level.