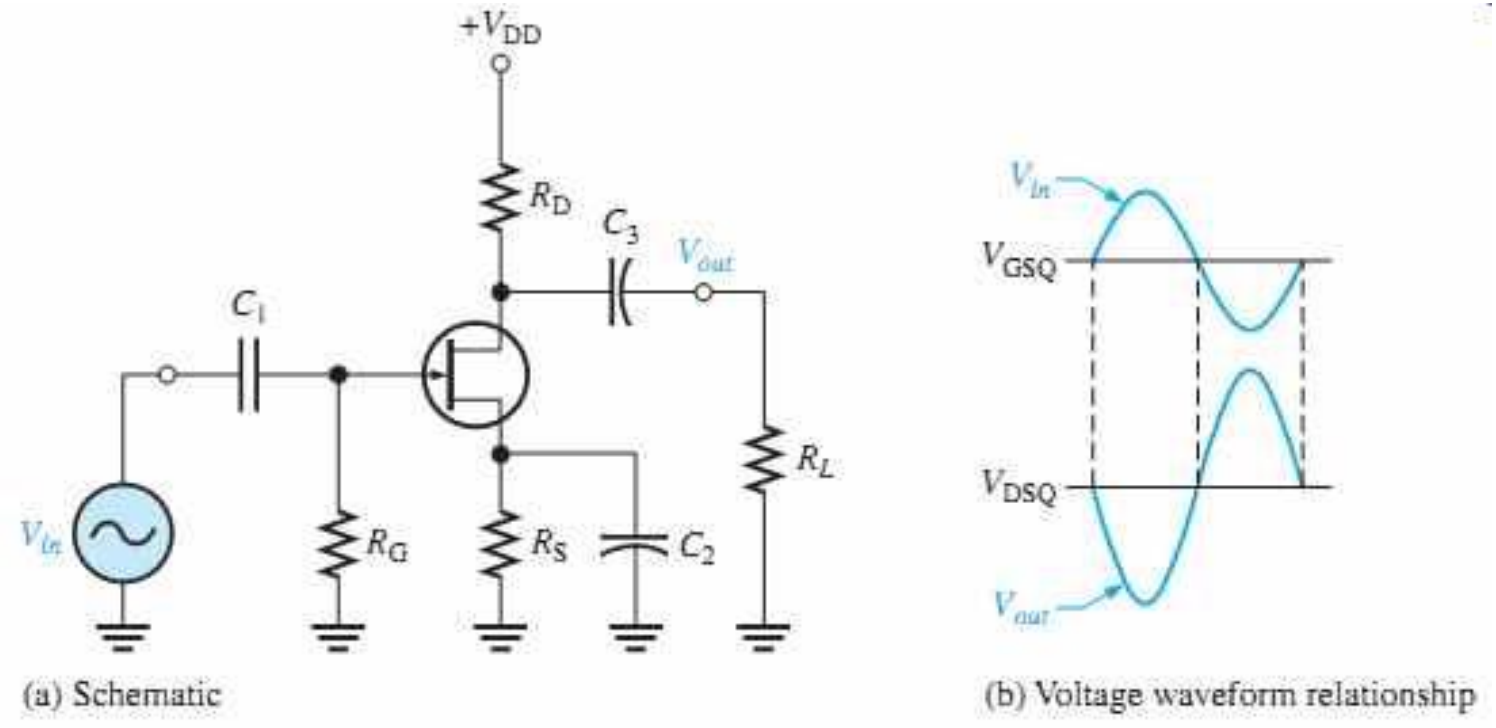
FET

JFET

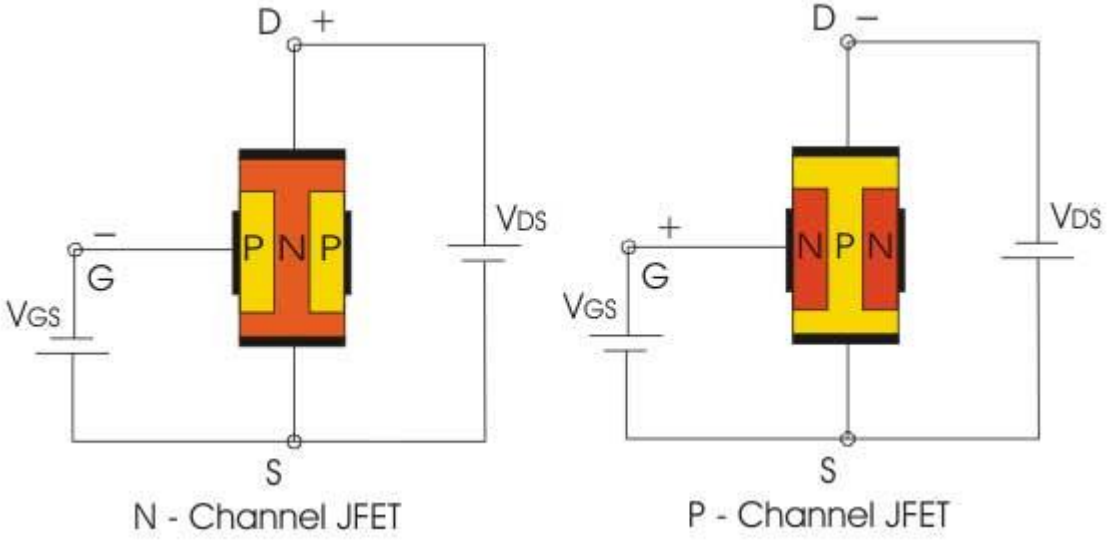
Circuito amplificador com JFET



(a) Schematic

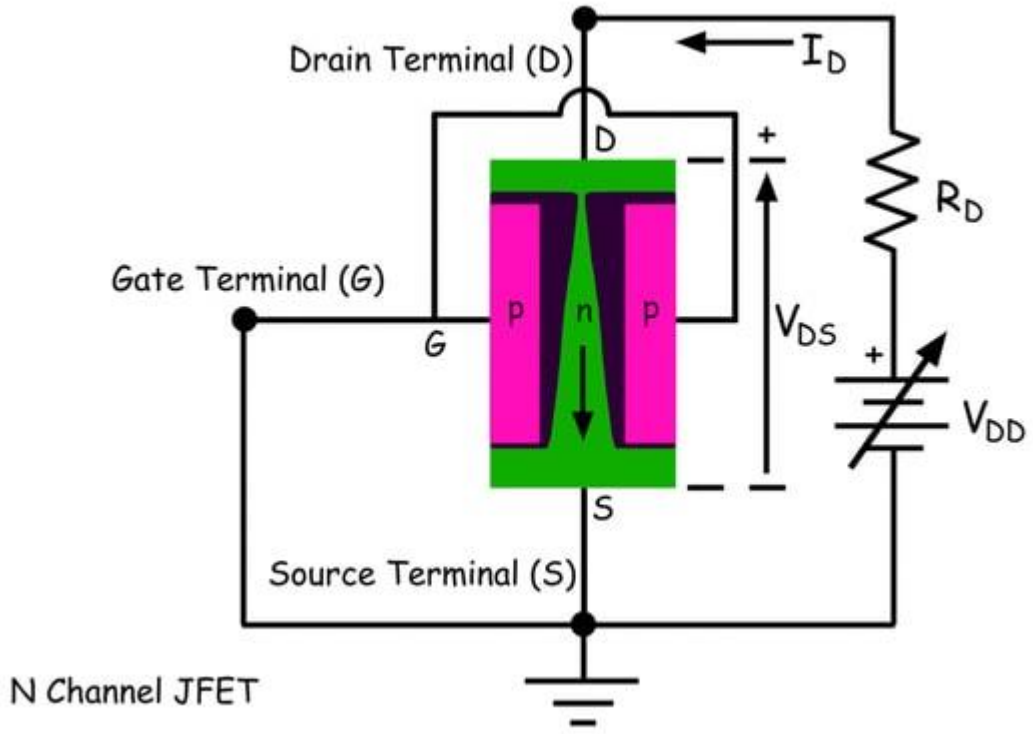
(b) Voltage waveform relationship

Junction Field Effect Transistor

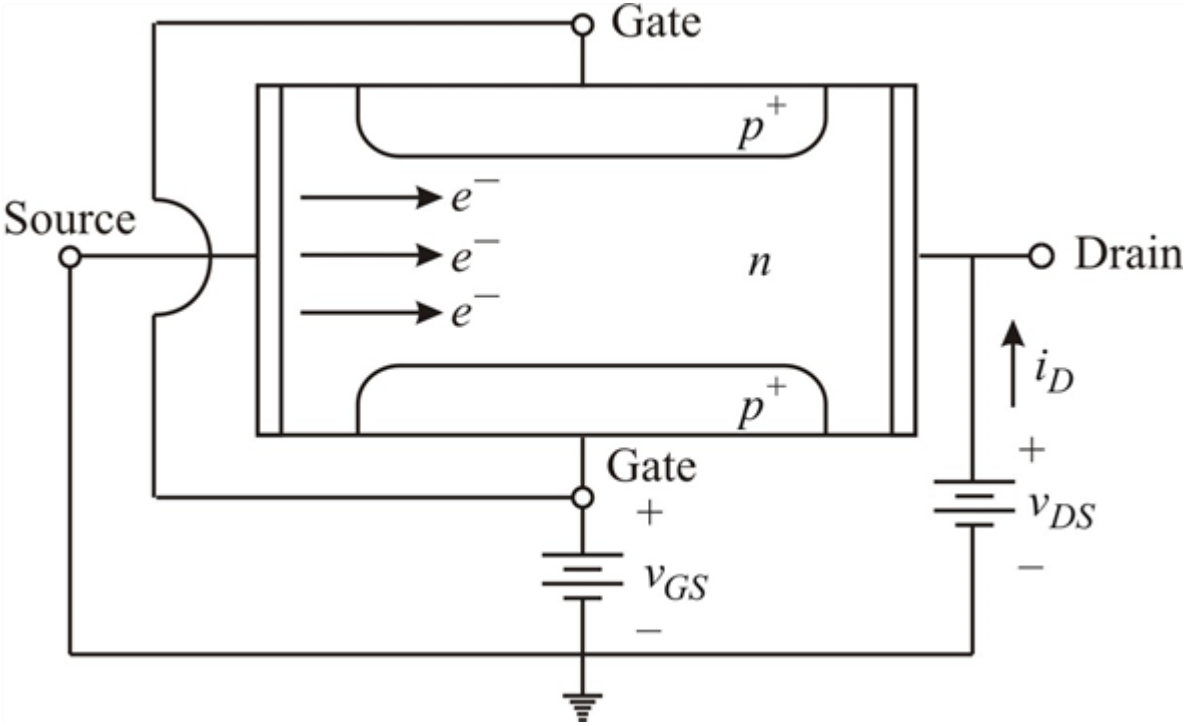


JFET

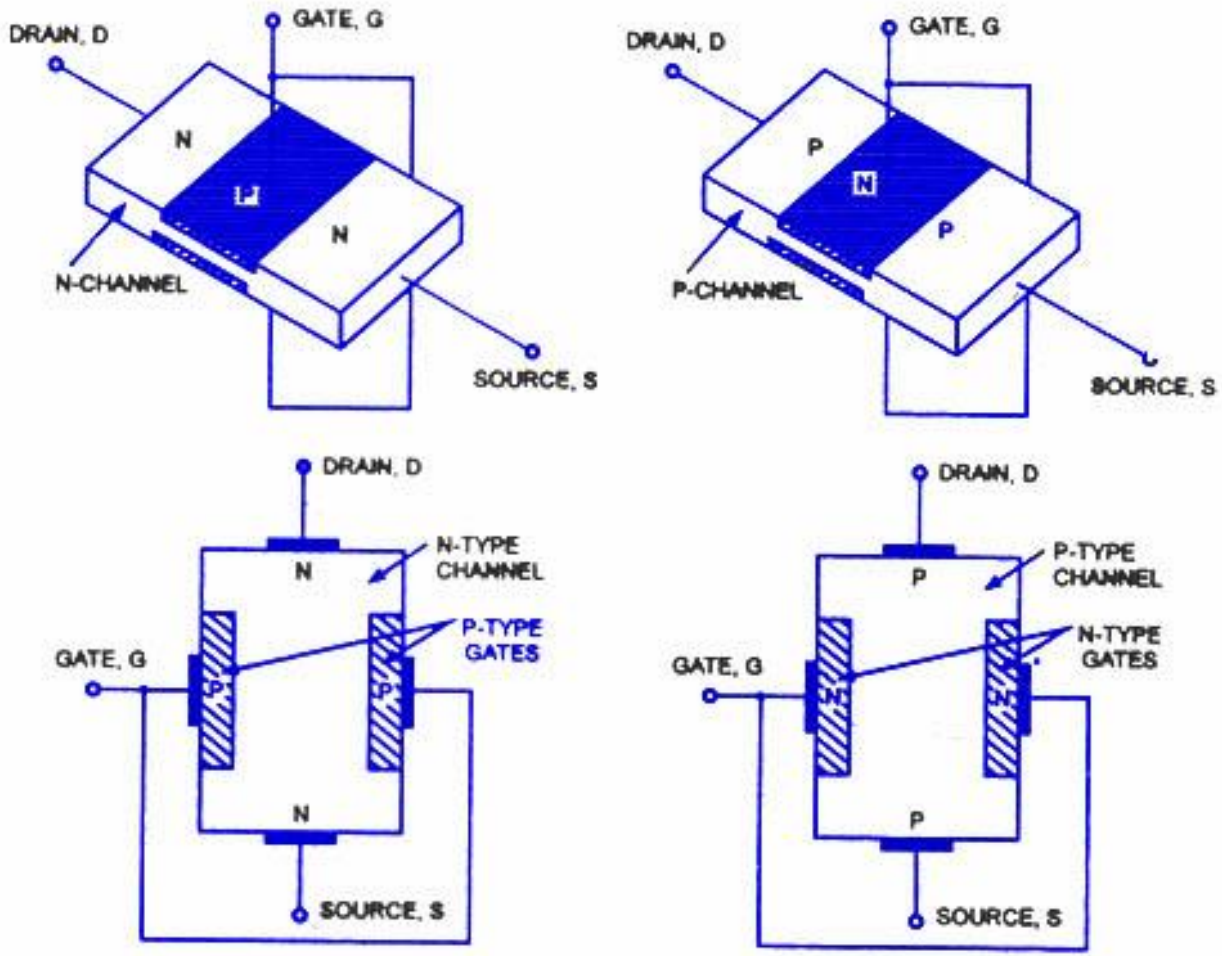
$$V_{GS} = 0$$


Drain Terminal (D)
I_D
D
+
R_D
Gate Terminal (G)
G
p
n
p
V_{DS}
+
V_{DD}
S
Source Terminal (S)
N Channel JFET

JFET



$$I_D = I_{DSS} \cdot \left(\frac{V_{GS}}{V_p} - 1 \right)^2$$

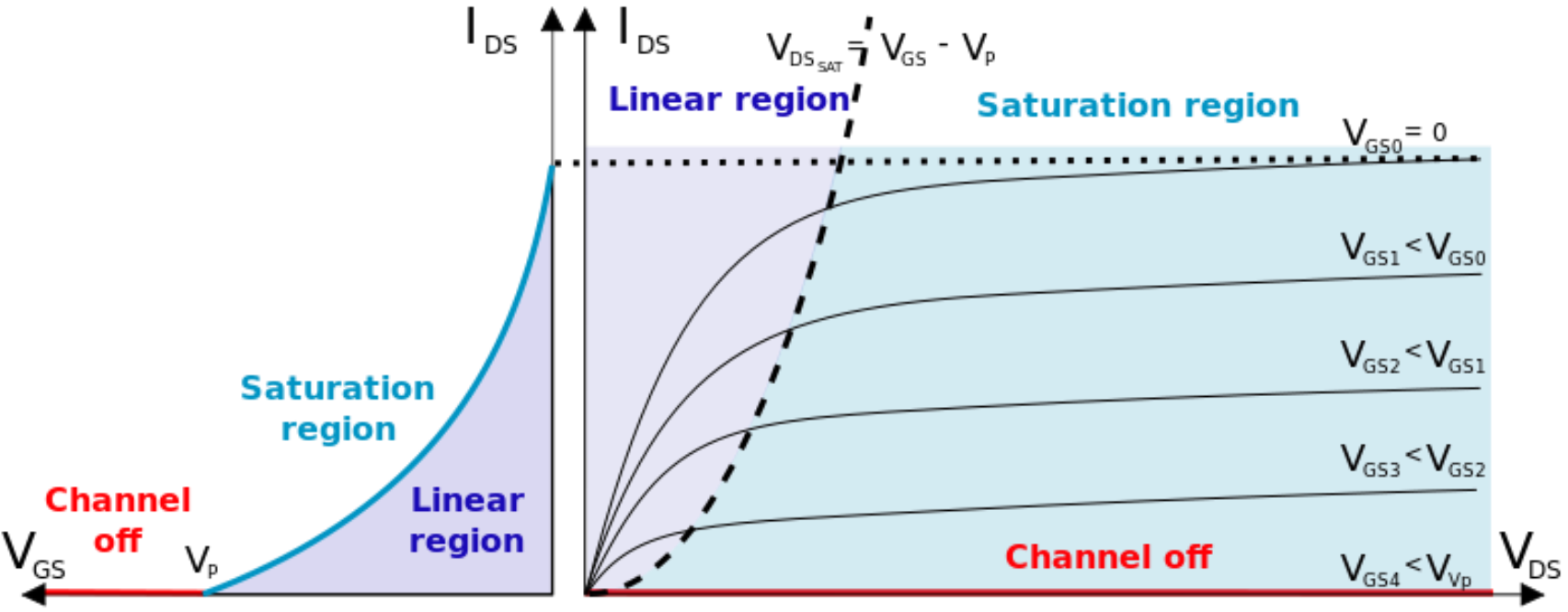


N-Channel JFET

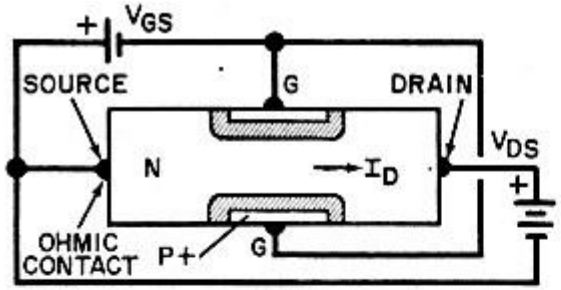
P-Channel JFET

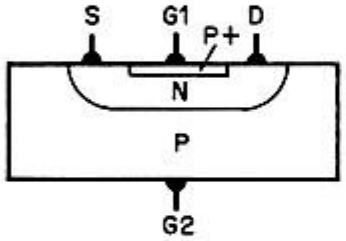
JFETs

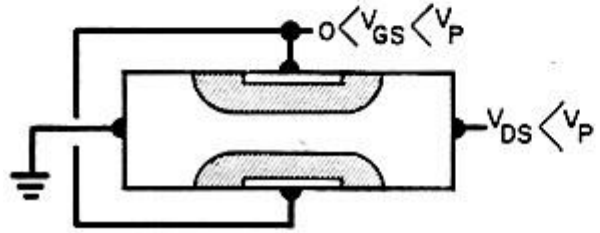
Curvas caracteristicas de entrada e saida de um JFET

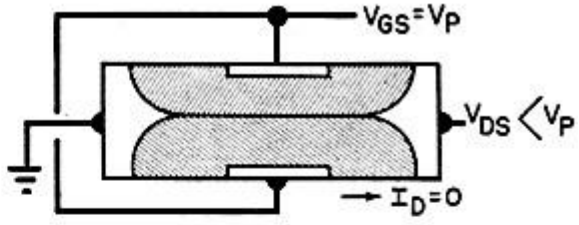


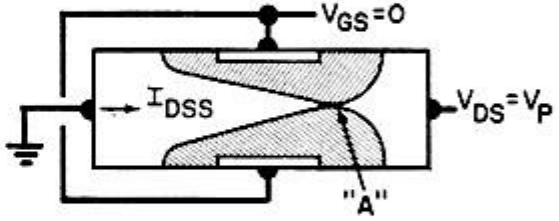
JFET

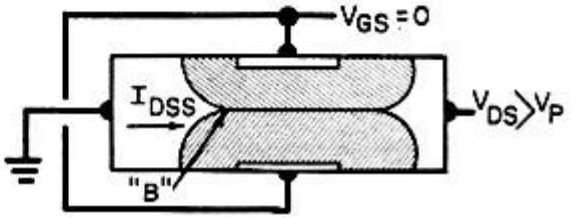

+
V_{GS}
SOURCE
G
DRAIN
N
I_D
V_{DS}
+
OHMIC CONTACT
P+
G
(A)


S
G1
P+
D
N
P
G2
(B)

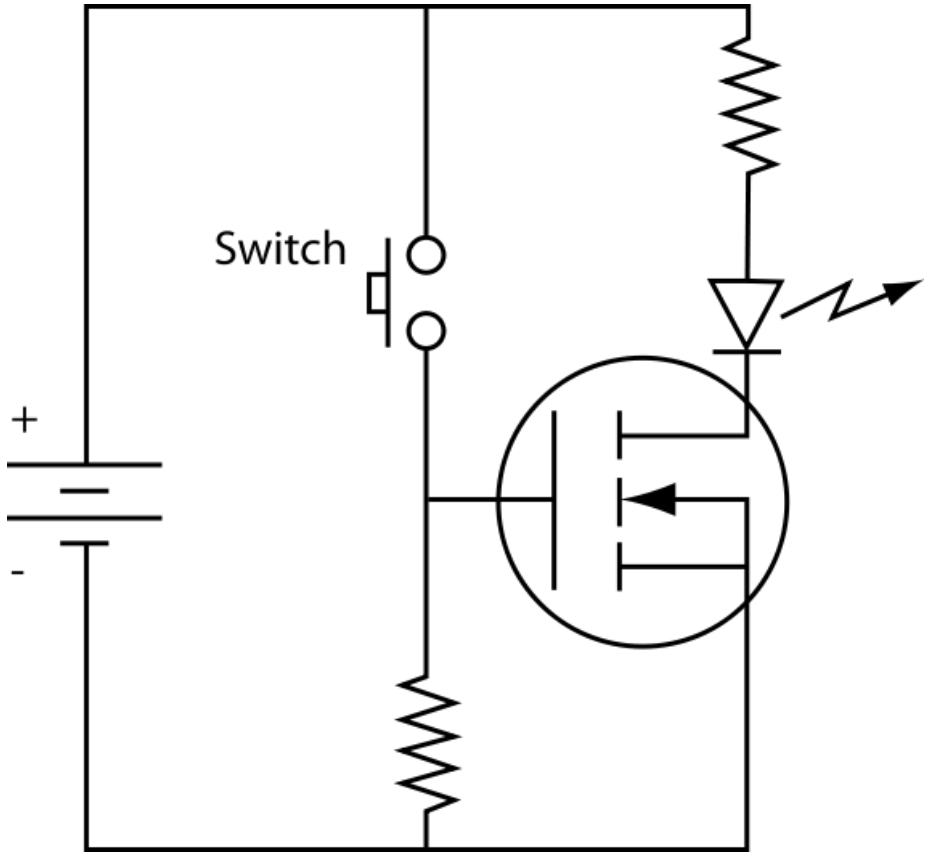

$0 < V_{GS} < V_P$
$V_{DS} < V_P$
(C)


$V_{GS} = V_P$
$V_{DS} < V_P$
$I_D = 0$
(D)

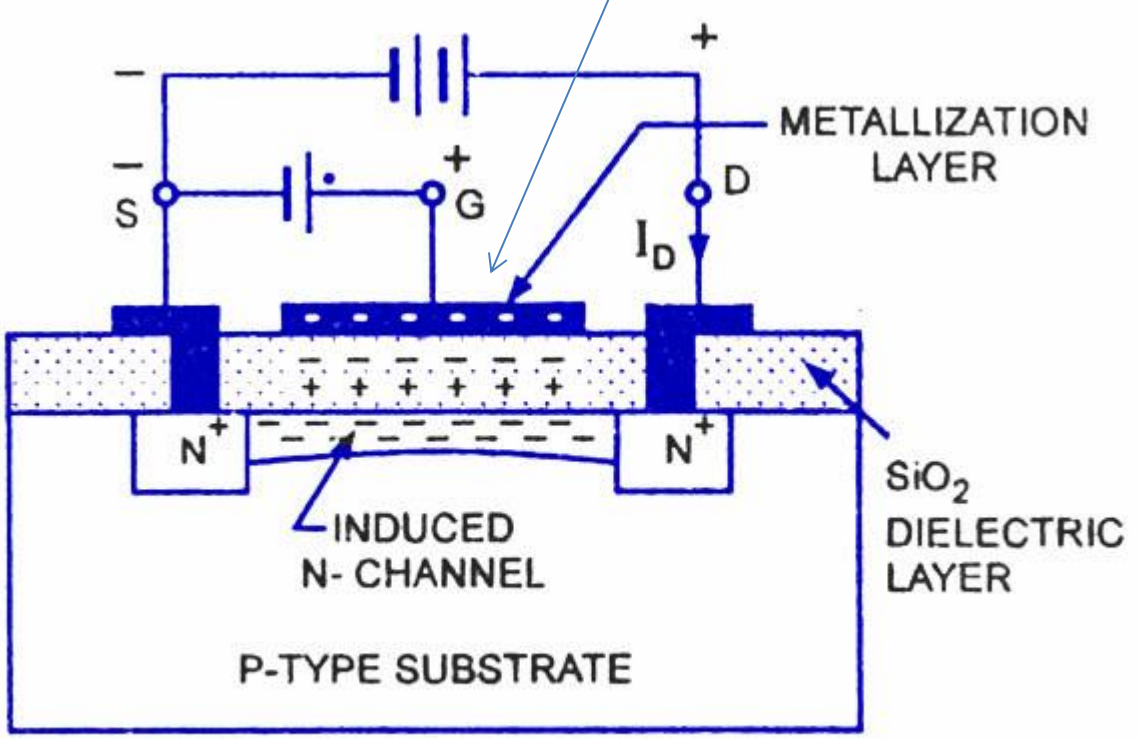

$V_{GS} = 0$
I_{DSS}
$V_{DS} = V_P$
"A"
(E)


$V_{GS} = 0$
I_{DSS}
$V_{DS} > V_P$
"B"
(F)

MOSFET

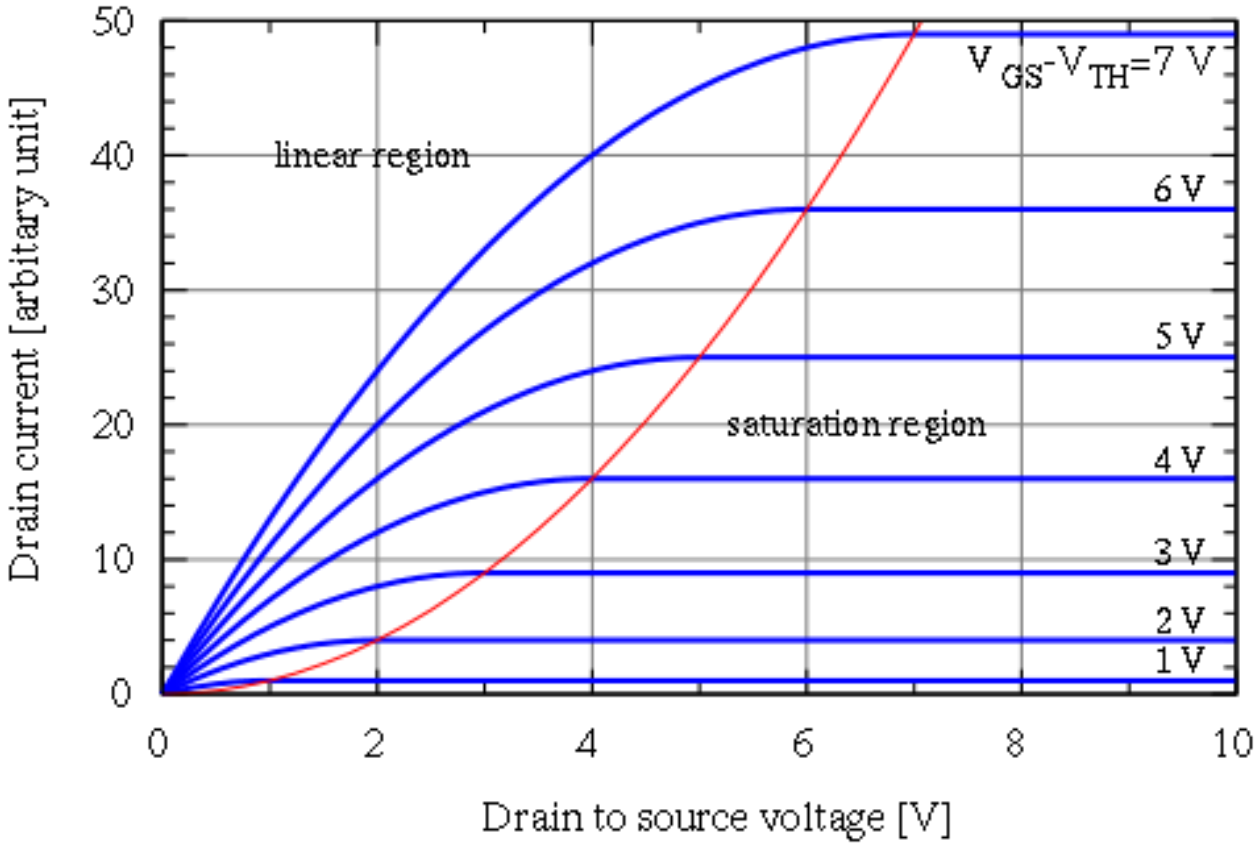


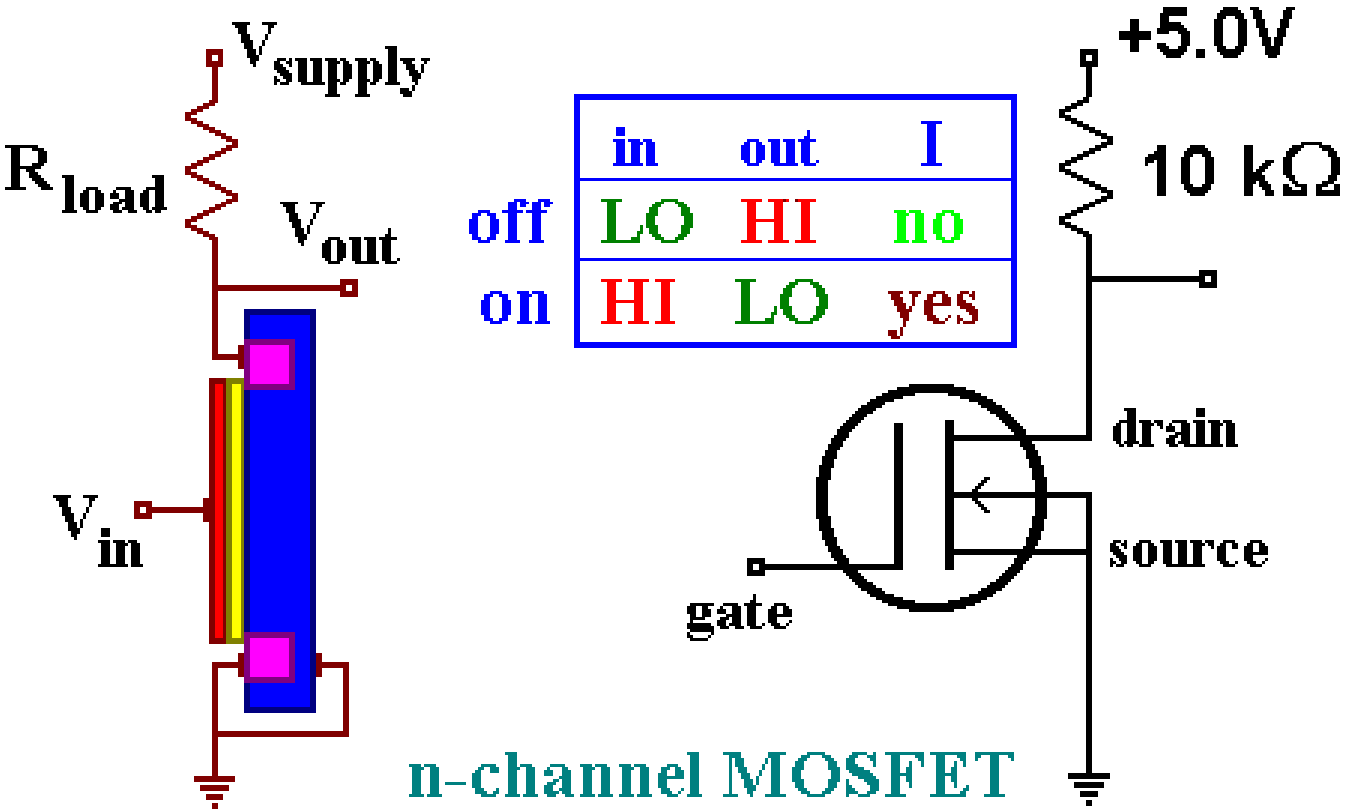
Positive +++



Operation of N-Channel E-MOSFET

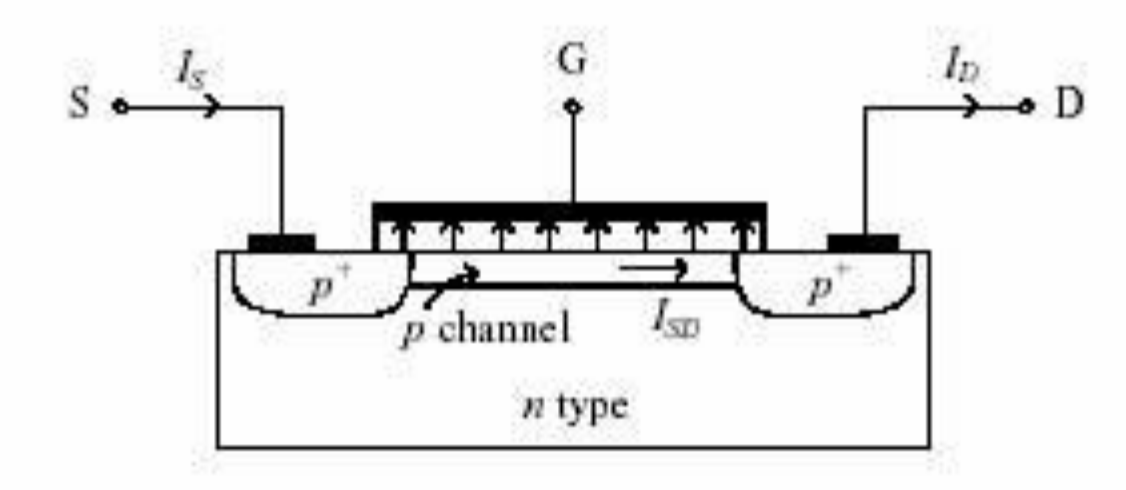
IDS versus VDS Curves



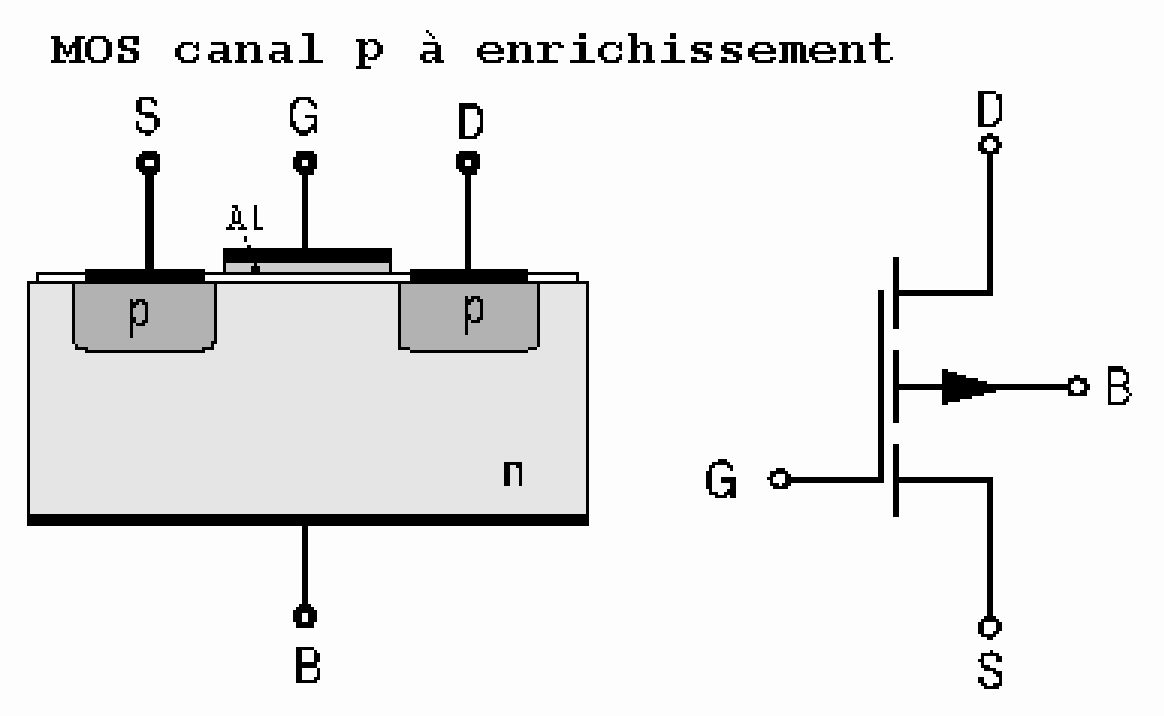


	in	out	I
off	LO	HI	no
on	HI	LO	yes

P channel MOS



P Channel MOS

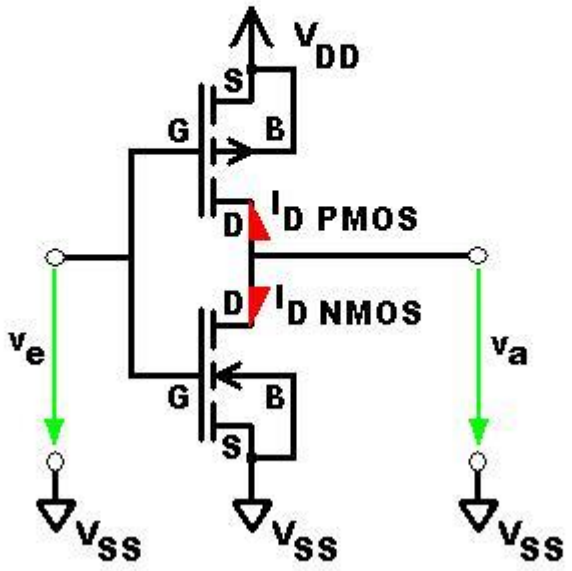


CMOS

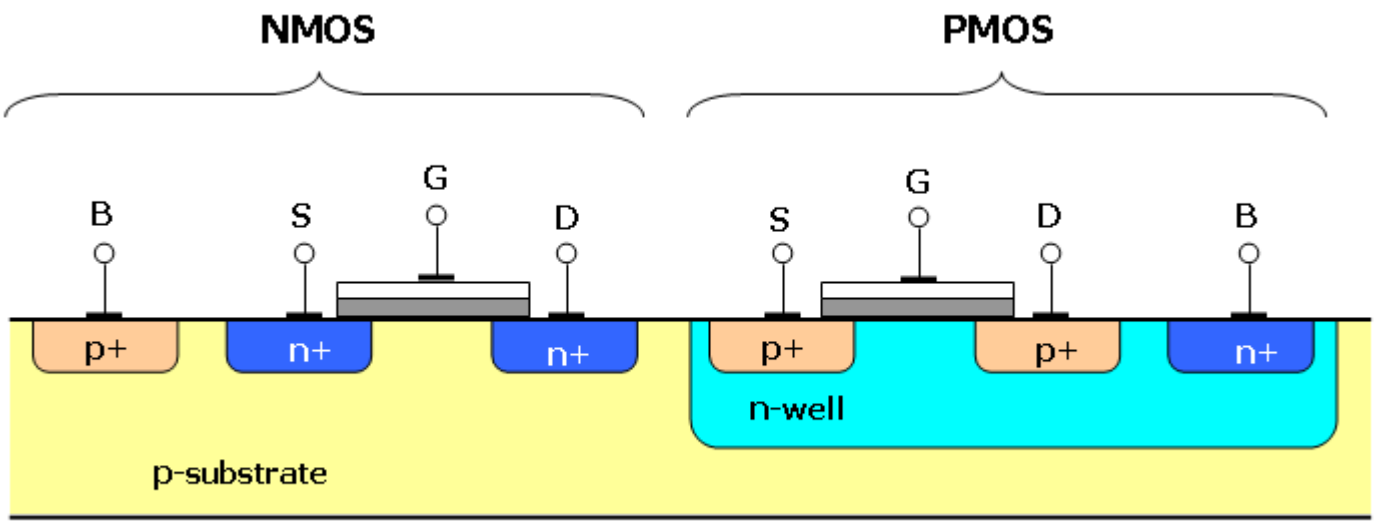
Drain / Source Gebiete am Beispiel CMOS Inverter

PMOS enhancement ($V_{TH} < 0$ V)

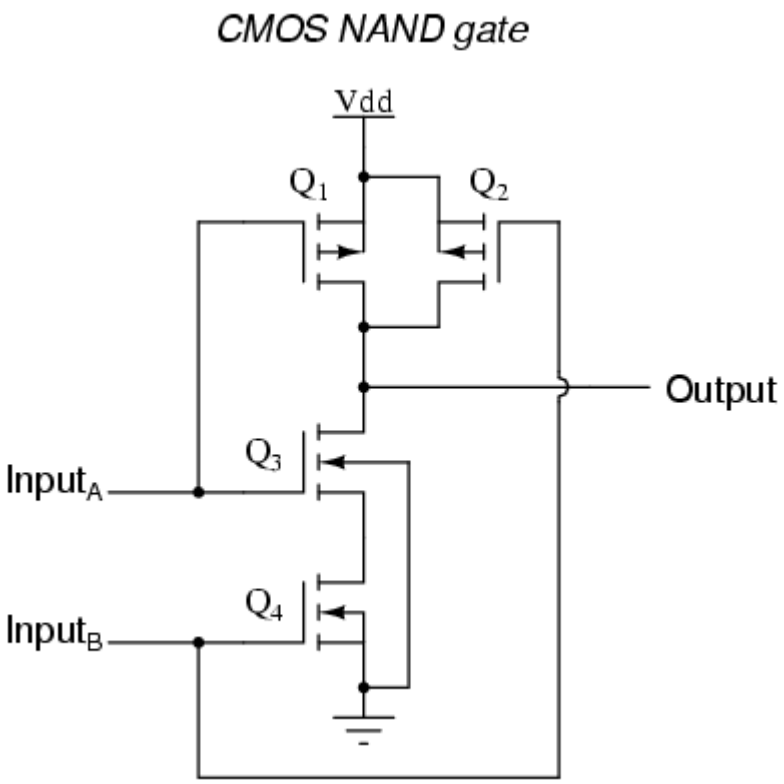
NMOS enhancement ($V_{TH} > 0$ V)

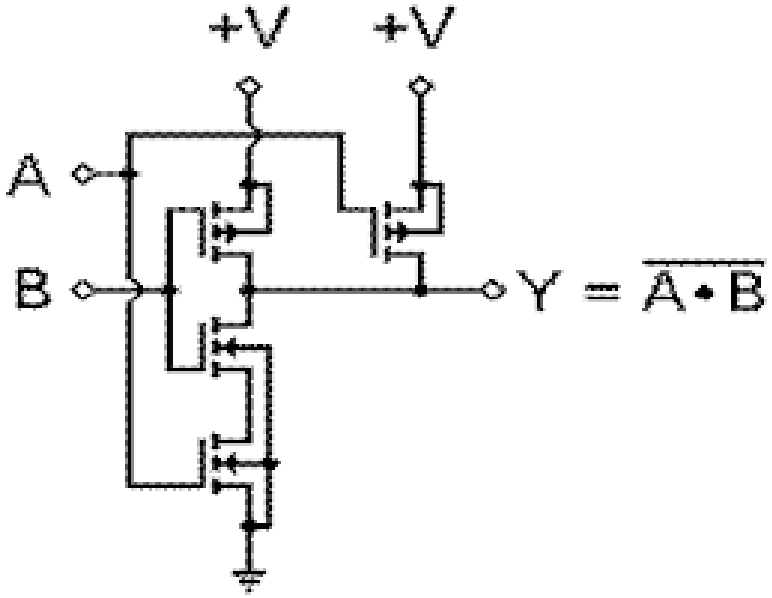


CMOS



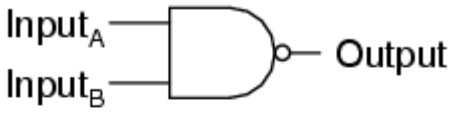
CMOS





CMOS Digital family

2-input NAND gate



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Equivalent gate circuit

FIM